Functional Analysis of Circuits Under Timing Variations

Mehdi Dehbashi*
*Institute of Computer Science
University of Bremen
28359 Bremen, Germany
dehbashi@informatik.uni-bremen.de

Görschwin Fey*†
†Institute of Space Systems
German Aerospace Center
28359 Bremen, Germany
goerschwin.fey@dlr.de

Kaushik Roy‡, Anand Raghunathan‡
‡School of Electrical and Computer Engineering
Purdue University
West Lafayette, IN 47907, USA
{kaushik, raghunathan}@purdue.edu

***Abstract*—This work proposes an approach to model and evaluate the functional behavior of logic circuits under timing variations. In the approach, first we construct a *Time Accurate Model* (TAM) of the circuit to represent its timing behavior in a functional domain under a discrete time model. Then, timing variations are applied by using *Variation Logic* (VL).**

I. Introduction

Timing variations are a major challenge in analyzing circuits as the feature sizes shrink down into the nanometer scale. Timing variations are caused by process uncertainty in the parameters of fabricated devices and by environmental effects such as temperature and voltage [1] [2]. On the one hand, recently there is a range of works on timing analysis of circuits under variations [1] [3]. On the other hand, there is a significant progress in the area of approximate computing which rely on bounded results but not necessarily exact results [4]. In [5], a methodology is presented to analyze an approximate circuit. However, the timing variations are not considered. In this paper, we present an approach to analyze a circuit under timing variations and timing-induced approximations (overclocking). First the timing behavior of a circuit is converted into the functional domain. Also, the circuit is enhanced by *Variation Logic* (VL) to model timing variation. Furthermore, a *Time Control* (TC) unit is added to control the clock period and to model timing-induced approximations like overclocking.

II. Approach

The underlying idea for modeling the timing behavior is to use copies of a gate to represent the value of a gate at different points in time. First an *original gate* g with delay n is converted to n successive *untimed gates*: $(g, Buf_{n-1}, \ldots, Buf_1)$. Each untimed gate has a delay of one time unit. Therefore, the timing behavior of the circuit with accuracy of one time unit can be evaluated. Then, if an untimed gate is exercised several times at different time steps (e.g. due to reconvergent fanout), one copy of the untimed gate in each related time step is created. The newly created gates are called *TAM gates* and constitute a new circuit called the *TAM circuit*. In this case, a TAM gate g_t represents an original gate g at time step t.

To model maximum timing variation D, first D additional copies of each TAM gate are created. Afterwards, multiplexers are added to the TAM gate outputs to model variations by selecting the signal value from different time steps. This part is called *Variation Logic* (VL). The select lines of the multiplexers are constrained to control the maximum timing variation D. Also, *Time Control* (TC) constrains a clock period T on the inputs with the accuracy of one time unit.

This work has been funded in part by the German Research Foundation (DFG, grant no. FE 797/6-1).

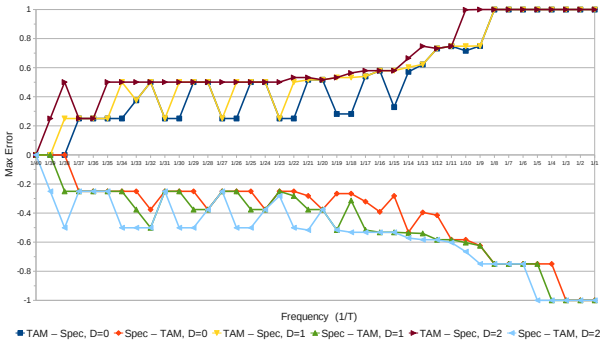

Fig. 1. Maximum error for 8-bit RCA

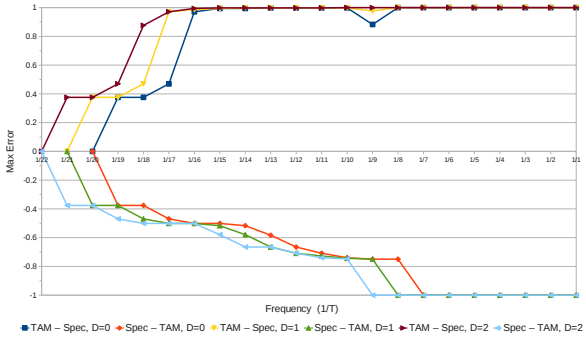

Fig. 2. Maximum error for 8-bit CLA

III. Experimental Results

We evaluate *Ripple Carry Adder* (RCA) and *Carry Look-ahead Adder* (CLA) benchmarks. A miter on the outputs of the specification and the TAM is used to measure the output deviation as the numerical difference. Figure 1 and Figure 2 show the maximum positive and negative error computed for an 8-bit RCA and an 8-bit CLA under overclocking and in the presence of timing variations. The X-axis indicates the frequency f as the inverse of the clock period T ($f = 1/T$). The Y-axis indicates the maximum error as a result of the computed error divided by the maximum output value.

References

[1] D. Blaauw, K. Chopra, A. Srivastava, and L. Scheffer, "Statistical timing analysis: From basic principles to state of the art," *IEEE Trans. on CAD of Integrated Circuits and Systems*, vol. 27, no. 4, pp. 589–607, 2008.

[2] M. Alioto, G. Palumbo, and M. Pennisi, "Understanding the effect of process variations on the delay of static and domino logic," *IEEE Trans. VLSI Syst*, vol. 18, no. 5, pp. 697–710, 2010.

[3] L. Xie and A. Davoodi, "Bound-based statistically-critical path extraction under process variations," *IEEE Trans. on CAD of Integrated Circuits and Systems*, vol. 30, no. 1, pp. 59–71, 2011.

[4] M. A. Breuer, "Hardware that produces bounded rather than exact results," in *Design Automation Conf.*, 2010, pp. 871–876.

[5] R. Venkatesan, A. Agarwal, K. Roy, and A. Raghunathan, "MACACO: Modeling and analysis of circuits for approximate computing," in *Int'l Conf. on CAD*, 2011, pp. 667–673.