System-Level Verification of Linear and Non-Linear Behaviors of RF Amplifiers using Metamorphic Relations

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ABSTRACT

System-on-Chips (SoC) have imposed new yet stringent design specifications on the *Radio Frequency* (RF) subsystems. The *Timed Data Flow* (TDF) model of computation available in SystemC-AMS offers here a good trade-off between accuracy and simulation-speed at the system-level. However, one of the main challenges in system-level verification is the availability of *reference models* traditionally used to verify the correctness of the *Design Under Verification* (DUV). Recently, *Metamorphic testing* (MT) introduced a new verification perspective in the software domain to alleviate this problem. MT uncovers bugs just by using and relating test-cases.

In this paper, we present a novel MT-based verification approach to verify the linear and non-linear behaviors of RF amplifiers at the system-level. The central element of our MT-approach is a set of *Metamorphic Relations* (MRs) which describes the relation of the inputs and outputs of consecutive DUV executions. For the class of *Low Noise Amplifiers* (LNAs) we identify 12 high-quality MRs. We demonstrate the effectiveness of our proposed MT-based verification approach in an extensive set of experiments on an industrial system-level LNA model without the need of a reference model.

1 INTRODUCTION

Analog circuits and *Radio Frequency* (RF) subsystems have become responsible for the largest fraction of the verification costs in a *System-on-Chip* (SoC) [20]. As a consequence methodologies are required to design, verify and produce high quality SoCs cost-effectively. In particular, analog/RF verification faces significant challenges due to the increasing stringent design complexity. A major challenge in analog/RF verification is the simulation speed of SPICE-level models [2]. Traditionally, SPICE-level simulations [18] are used often with manual inspection of the results. These simulations, while slow, are still considered a golden standard and cannot be ignored. However, different levels of design abstractions can be used to achieve significantly better simulation performance, and earlier design verification of the *Design Under Verification* (DUV).

As a consequence, *Virtual Prototyping* (VP) at the abstraction of *Electronic System Level* (ESL) is nowadays an established practice [8, 11, 12, 19, 25]. The *Timed Data Flow* (TDF) *Model of Computation* (MoC) available in SystemC-AMS offers a good trade-off between accuracy and simulation-speed at the SoC level. TDF defines time domain processing, and is used to model the pure algorithmic or procedural description of the underlying design. Because of earlier availability and significantly faster simulation speed as opposed to SPICE-level simulations [2], the TDF models provide a design refinement methodology and enable early verification for analog/mixed-signal systems[1] [9, 10]. Hence, their functional correctness is of utmost importance.

However, one of the main challenges is the availability of *reference models* for verification. When speaking about reference models we broadly cover approaches like co-simulation (for instance with Matlab/Simulink), or advanced testbench concepts based on the *Universal Verification Methodology* (UVM), and in the future even more abstract based on *Portable Stimulus Specification* (PSS). Regardless of the specific solution significant effort is needed to specify the reference behavior in an executable way.

Recently, a new verification perspective has been introduced in the software domain: *Metamorphic Testing* (MT) [5, 22, 23] which alleviates this problem. Instead of relying on the reference value computed from reference models, MT looks at *Metamorphic Relations* (MRs), i.e. how the inputs and outputs of multiple DUV executions relate. For example, consider a DUV that implements a ***sum*** function for adding two numbers. A MR can be $10 \times sum(2, 5) = sum(10 \times 2, 10 \times 5)$, where the first execution of *sum* (*Left Hand Side* (LHS) of the MR) has the inputs 2 and 5 (termed base test-case), and the second execution (*Right Hand Side* (RHS) of the MR) has the inputs 10×2 and 10×5 (termed follow-up test-case). Instead of verifying what the output of each execution would be, MT only checks if both sides of the MR are equal, i.e. the DUV output of first execution when multiplied by 10 should equal the DUV output of second execution. If the MR is not satisfied, i.e. $LHS \neq RHS$, MT has found a bug. Furthermore, each MR inherently creates follow-up test-cases using successful base test-cases. Employing MT, a large-number of real-life faults have been found in complex software where reference models have not been available, see e.g. [6, 13, 24].

Contribution: In this paper, we propose a MT-based verification approach to effectively verify the linear and non-linear behaviors of RF amplifiers at system-level. As a representative of RF amplifiers

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[1]Visit http://www.systemc-verification.org/ams for our most recent approaches.

we consider *Low Noise Amplifiers* (LNAs). Before we present our MT-approach in detail, we introduce a high-quality set of 12 MRs for the class of RF amplifiers. As reference models are not required to ensure correctness when performing MT, the investment to use the proposed MT-approach is low. However, the potential benefit in design verification is huge. In an extensive set of experiments on an industrial configurable system-level LNA model, our proposed MT-approach found a serious bug which escaped during the regular verification process. Furthermore, we perform a fault-injection campaign on the industrial LNA to demonstrate the fault-detection quality of our MT-based verification approach. We show that our MT-based verification approach successfully verifies the linear and non-linear behavior of the LNA without the need of a reference model.

Summarizing the main contributions of this paper are:

- Novel MT-based verification approach for AMS verification at system-level
- High-quality set of MRs (applicable for all variants of RF amplifiers)
- Demonstration of MT-effectiveness on industrial LNA model without the need of reference models

2 RELATED WORK

Metamorphic relations (introduced in detail in Section 3) are the core element of metamorphic testing and differ from properties as defined and used in classical verification environments in the AMS domain, such as [7, 14, 17]. In [17], a property-based monitoring framework for AMS systems is presented. The properties are defined using *Signal Temporal Logic* (STL) specification language and implemented using assertions. STL allows describing complex timing relations between digital and analog "events" , where the latter are specified via numerical predicates. While a great initiative, it requires a significant learning curve and the expected output has to be known (and is put into the property accordingly).

[14] introduces the *Language for Analog/Mixedsignal Properties* (LAMP) to provide AMS designers with a more intuitive and easier to use property language. It uses *Petri Nets* to model circuits and then verifies the properties on them. It provides a set of functions that can be automatically compiled in to a property. However, as above the expected behavior has to be specified explicitly.

[7] is concerned with making the monitoring of simulations more efficient and reliable, and as automatic as possible. It is centered around a formalism for specifying requirements, expected properties and performance measures that can be the basis for automatic monitoring, liberating the engineers from these tedious tasks. However, the authors always use specifications to create the properties.

With the particular focus on system-level modeling and SystemC/AMS, [3, 21] use *Assertion Based Verification* techniques to verify the digital and analog/mixed-signal systems. However, all the approaches rely on the reference models for assertion definition.

In contrast to the aforementioned works, we propose an approach based on MRs which, instead of looking at a particular behavior of a signal or specifications of the DUV, allows the verification without explicit reference descriptions.

Closest to our work is [16] since MT is considered in the context of hardware. However, this work targets the problem of digital hardware fault-tolerance and not AMS verification.

3 METAMORPHIC TESTING FOR RF AMPLIFIERS

First, we present how to transfer the MT principles to the domain of RF amplifiers. Then, we identify generic MRs as basis for our overall MT-approach which is introduced in Section 4.

3.1 MT Principle for RF Amplifiers

To leverage MT for verification of RF amplifiers, the central element of MT, i.e., set of MRs, has to be identified. Recall that a MR is a necessary property of the target function (so in our case an RF amplifier) in relation to multiple inputs and their expected outputs. Linearity of an RF amplifier is one such property where the RF amplifier increases the power level of an input signal without altering the content of the signal. We demonstrate the MT principle for RF amplifier with an example. Let's consider a concrete RF amplifier and its behavior, that is defined as $output = 7 \times input$, i.e., the amplifier input is amplified by 7 times (gain factor of 7). To verify the RF amplifier functionality, the linearity property is converted to the following concrete MR: $3 \times Amp_{vout}(x(t)) = Amp_{vout}(3 \times x(t))$.[2] The MR states that the output voltage of the first execution scaled by a factor of 3 should always equal to the output voltage of the second execution with an input scaled with a factor of 3. Let's consider this graphically: The base test-stimulus $x(t) = sin(2\pi 5000t)$ is shown in Fig. 1a and the corresponding output signal is shown in Fig. 1b, which is 7 times $x(t)$, i.e. $7 \times sin(2\pi 5000t)$. The output signal of the follow-up test stimulus $3 \times x(t) = 3 \times sin(2\pi 5000t)$ (Fig. 1c) is shown in Fig. 1d. According to the MR from above, it should hold now that $3 \times Amp_{vout}(x(t))$, i.e. 3× Fig. 1b, equals Fig. 1d which is $Amp_{vout}(3 \times x(t))$. This is obviously satisfied here. In case, the MR does not hold, the amplifier is termed buggy.

In the next section we generalize this principle and identify 12 MRs for RF amplifiers as basis for proposed MT-approach.

3.2 Identification of Metamorphic Relations

Before we introduce the MRs, we outline the conventions that will be used for all MRs detailed in the text below. We have a function $f(x(t))$ defined in Eq. 1 as

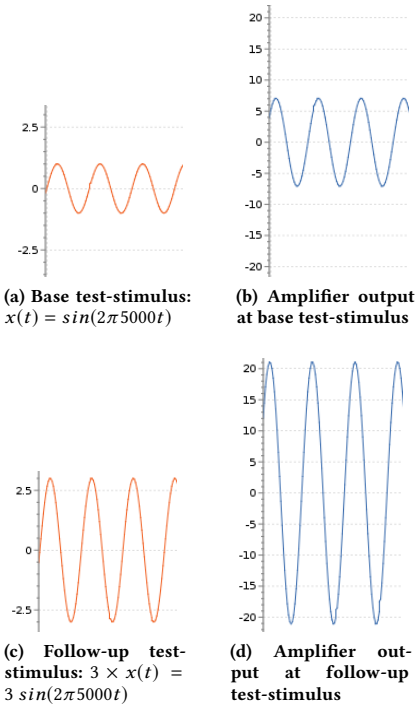
$$f(x(t)) = Amp_{char}(x(t)) \qquad (1)$$
$$x(t) = A\, sin(2\pi Ft + \varphi)$$

where Amp_{char} is the amplifier output for a characteristic *char* at an input signal $x(t)$, A is the amplitude, F is the frequency, and φ is the phase of $x(t)$. For future references, $x(t)$ will be used as x interchangeably. *char* can be any one of the following:

$$char = \begin{cases} pout & \text{output power of amplifier (dBm)} \\ gain & \text{gain of amplifier (dB)} \\ vout & \text{output signal voltage (V)} \\ freq & \text{output signal frequency (Hz)} \end{cases}$$

Additionally, the transfer characteristics of amplifiers vary at small-signal levels and high power levels, and as a consequence, the MRs should be developed taking this behavior into account.

[2] We use here the concrete amplitude factor of 3 which is generalized later.



(a) Base test-stimulus: $x(t) = sin(2\pi 5000t)$

(b) Amplifier output at base test-stimulus

(c) Follow-up test-stimulus: $3 \times x(t) = 3\ sin(2\pi 5000t)$

(d) Amplifier output at follow-up test-stimulus

Figure 1: Graphical illustration of MR for amplifier *output* $= 7 \times$ *input*

Here, we present some of the identified MRs for both the linear and non-linear operating regions.

MR1: The output voltage of the RF amplifier scales by the same factor with which the input voltage is scaled. Let x_1 be the base test-case, x_2 is a follow-up test-case, and N is the scaling factor, where $x_2 = N \times x_1$, such that both signals are driving the amplifier in linear region, then the following should always hold

$$N \times Amp_{vout}(x_1) = Amp_{vout}(x_2)$$

MR2: The output voltage corresponding to the sum of any two input signals is the sum of the two outputs. If x_1 is a base test-case and x_2 is a follow-up test-case such that both signals drive the amplifier linearly then the following should always hold

$$Amp_{vout}(x_1 + x_2) = Amp_{vout}(x_1) + Amp_{vout}(x_2)$$

MR3: The output power of the amplifier at x_1 will always be lower than the output power of the same amplifier at x_2. If x_1 is a base test-case and x_2 is a follow-up test-case such that $x_1 < x_2$, and both the signals drive the amplifier in linear region, then the following should always hold

$$Amp_{pout}(x_1) < Amp_{pout}(x_2)$$

MR4: The output power of the amplifier at x_1 will always be greater than the output power of the same amplifier at x_2. If x_1 is a base test-case and x_2 is a follow-up test-case such that $x_1 > x_2$, and both the signals drive the amplifier in linear region, then the following should always hold

$$Amp_{pout}(x_1) > Amp_{pout}(x_2)$$

MR5: The amplifier gain should be constant for a range of input signals. If x_1 is a base test-case and x_2 is a follow-up test-case, such that both signals drive the amplifier linearly then the following should always hold

$$Amp_{gain}(x_1) = Amp_{gain}(x_2)$$
$$\forall\ x_1 < x_2, x_1 > x_2$$

MR6: The output power of amplifier should be constant for a range of input signals. If x_1 is a base test-case and x_2 is a follow-up test-case such that both x_1 and x_2 are very high and the amplifier is operating in saturation, then the following should hold

$$Amp_{pout}(x_1) = Amp_{pout}(x_2)$$
$$\forall\ x_1 < x_2, x_1 > x_2$$

MR7: The amplifier gain should decrease as the input signal power increases, for a range of input signals. If x_1 is a base test-case and x_2 is a follow-up test-case, where x_1 and x_2 are very high and the amplifier is operating in saturation, then the following should hold

$$Amp_{gain}(x_1) > Amp_{gain}(x_2)$$
$$\forall\ x_1 < x_2$$

MR8: All the harmonic distortions of the RF amplifier should shift as the input signal frequency increases. If x_1 is a base test-case with frequency F_1 and it results in output harmonics at F_1, $2F_1$, $4F_1$. The signal x_2 is a follow-up test case with $F_2 = N \times F_1$, then the following should hold

$$Amp_{freq}(x_2) = Amp_{freq}(x_1(NF_1)) + Amp_{freq}(x_1(2NF_1)) + Amp_{freq}(x_1(4NF_1))$$

MR9: Third-order IMD can cause interference to the desired signal frequencies (F_1 and $F_1^{'}$) because their products are higher in magnitude and close to the desired frequencies. Let x_1 be a two-tone base test-case with signal frequencies F_1 and $F_1^{'}$, where $F_1^{'}$ is slightly lower/higher than F_1. The third-order IMD for x_1 lies at $2F_1 - F_1^{'}$ and $2F_1^{'} - F_1$. Let x_2 be a two-tone follow-up test-case with frequency $F_2 = N \times [F_1 + F_1^{'}]$, i.e., the frequencies of x_1 are scaled by a factor of N. Then, the following should hold

$$Amp_{pout}(x_2) \cong Amp_{pout}(x_1)$$

MR10: The triple-beat test refers to three-tone, third-order IMD and holds a significant place in amplifier verification. Three-tone IMD involves terms of the form $F_1 \pm F_1^{'} \pm F_1^{''}$. If x_1 is a two-tone base test-case with frequencies $F_1 + F_1^{'}$ and the signal x_2 with frequencies $F_1 + F_1^{'} - F_1^{''}$ is a follow-up test-case, then the three-tone third-order IMD is 6 dB higher than two-tone third-order IMD [26] , and the following should always hold

$$Amp_{pout}(x_2) = Amp_{pout}(x_1) + 6dB$$

MR11: The fundamental principle of TOI is that for every 1 dB increase in the power of the input tones, the third-order products will increase by 3 dB on the output. If x_1 is a base test-case and $x_2 = x_1 + 1\ dB$, $x_3 = x_2 + 1\ dB$ are follow-up test-cases, such that $Amp_{pout}(x_1)$ gives third-order IMD from x_1 [26], then

$$Amp_{pout}(x_1) + Amp_{pout}(x_2) + Amp_{pout}(x_3) = 3 \times Amp_{pout}(x_1) + 9\ dB$$

MR12: If x_1 is a base test-case with power P_{x1dBm} and x_2 is a follow-up test-case with power P_{x2dBm}, then the difference in power at input should equal difference in power at output, i.e.,

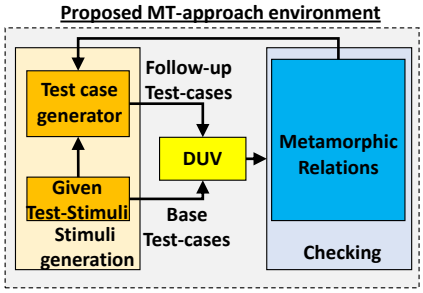


Figure 2: High-level block diagram of the proposed MT-based verification approach

$$P_{x2dBm} - P_{x1dBm} = Amp_{pout}(x_2) - Amp_{pout}(x_1)$$

Please note, the proposed MRs do not represent a complete set of MRs for the amplifiers by any means and more MRs can be identified in principle.

4 MT-BASED SYSTEM-LEVEL VERIFICATION APPROACH

In this section we present our MT-based verification approach for the verification of linear and non-linear behaviors of RF amplifiers. We use the developed MRs to verify the DUV correctness without the need of reference models. First, we present an overview describing the main components. Afterwards, the different components are briefly explained.

4.1 Overview

A high-level block diagram of the proposed MT-based verification approach is shown in Fig. 2. It consists of two major components: *Stimuli generation* and *Checking*. *Stimuli Generation* uses the given test-stimuli, i.e., test-stimuli used during the regular verification process, and MRs to generate follow-up test-cases. The given test-stimuli and the follow-up test-stimuli are input to the DUV to exercise different linear and non-linear behaviors of the model. The *Checking* block collects DUV outputs for performing relation checks, i.e., comparison of LHS and RHS according to the MRs. In the next sections, we briefly explain the components of our approach.

4.2 Stimuli Generation

As shown in Section 3.1, MRs require multiple executions of the DUV with varying inputs. Hence, multiple test-stimuli are required which build on top of a base test-stimuli. Therefore, the selection of base test-stimuli is of utmost importance because it lays the foundation of the follow-up test cases. The test-stimuli from the verification plan created during the regular verification process are a good candidate as a base test-stimuli. Therefore, we use them as base test-stimuli.

4.3 Checking

The base test-cases and the follow-up test-cases exercise the linear and non-linear behaviors of the DUV. Verification of the correct DUV behavior is carried out in the *Checking* block. As motivated earlier, MRs don't need reference models. Hence, the *Checking* block performs relation checks, i.e. compares the LHS and the RHS of MRs. If both the sides of the MR are equal, the MR passes, otherwise it fails.

The investment to use the MT-based verification approach is low. However, the potential benefit in design verification is huge. In the next section we present an extensive set of the experiments on an industrial system-level model using the MT-based approach.

5 EXPERIMENTS

In this section we present the experiments to demonstrate the effectiveness of our approach for the verification of linear and non-linear behaviors of RF amplifiers. For the experiments we use a configurable system-level model of an LNA provided by our industrial collaboration partner. Section 5.1 provides the details on the LNA model (including the different possible configurations) as well as the experimental setup. Then, Section 5.2 presents the verification results obtained with the proposed MT-approach. We have found a serious bug in the LNA using the presented MRs, which escaped during the extensive verification performed by our industrial partner. Finally, we show in Section 5.3 the general quality of our MT-approach for verification. For this, we perform a fault-injection campaign on the LNA model and demonstrate that the developed MRs are able to detect all injected faults without the need of a reference model.

5.1 LNA Model and Experimental Setup

In general, an LNA amplifies a weak low power input signal without affecting its *Signal-to-Noise-Ratio* (SNR) significantly. LNAs can be found in various applications in RF front-ends, e.g. mobile phones, automotive keyless entry devices, Wireless LANs etc. In this paper, we consider as DUV a system-level industrial LNA model, denoted as *I_LNA* in the following. It is a behavioral model and has been implemented by our industry partner using the well-known concepts from [4, 15]. The specific configuration of the *I_LNA* adheres to the following specifications:

- *Gain* (G) (min., typical, max.) = 16.5 dB, 18.2 dB, 20 dB
- Input signal amplitude = 0 V to 2 V.
- 1 dB compression point = 30 dBm
- Output *Third-Order Intercept* (IP3) = 70 dBm
- Operating frequency = 5 KHz to 20 KHz
- Input impedance = 50 Ohms
- Output impedance = 50 Ohms

The *I_LNA* has been implemented in SystemC-AMS as an abstract static non-linear description as a TDF model. The model comes with a set of test-stimuli created according to the verification plan, i.e. an intensive verification of the linear and non-linear behaviors of the *I_LNA* has already been performed by our industrial partner. Hence, they do not expect any faults in the model.

5.2 MT-based Verification Results

In this experiment, we use the test-stimuli of the *I_LNA*, which have been shipped together with the model as mentioned in the previous section. The standard RF specifications of interest have been *gain*, *1dB compression point*, and the intercept points – *Input Second/Third Order Intercept* (IIP2/3). As expected the RF specifications have been verified with the given test-stimuli and no faulty behavior was observed. The linear and non-linear behaviors were correct. At this point we employed our MT-approach using the given test-stimuli

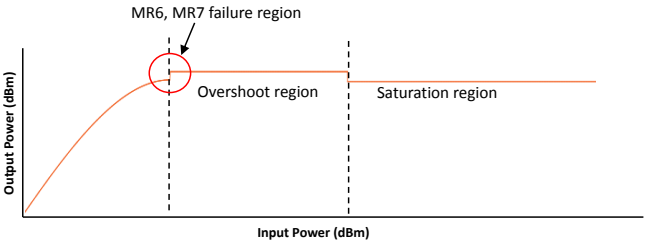


Figure 3: *I_LNA* Ouput power vs Input power (dBm). Overshoot of output power because of non-linearity approximation.

as the base test-cases. The follow-up test-cases were created with our MT-approach based on the MRs from Section 3.2. Hence, without any manual effort our MT-approach immediately found the violation of two MRs: **MR6** and **MR7** failed. The output power and the corresponding gain of *I_LNA* did not follow the *core properties* of the LNA, reflected in these MRs. At higher input voltage, the LNA saturates and the output power should become constant and the corresponding gain value should decrease in successive test-cases. However, the *I_LNA* did not show this behavior (check **MR**6, **MR**7 Section 3.2). Upon close manual inspection of the waveform (Fig. 3, we observed a slight overshoot of the gain curve for a short duration before settling to a stable value in the saturation region. This faulty behavior is easy to miss and requires test-cases in a certain range of values to exercise this behavior. However, with the proposed MRs, the follow-up test-cases are computed at no additional cost and even helps to debug the model: Based on both failed MRs and the created follow-up test-case, we saw that the amplitude was increased which drove the amplifier in the non-linear region. In this region the underlying approximation algorithm used in *I_LNA* could not handle this non-linearity properly. As a consequence, the gain did not converge and hence the relation check (comparison of LHS and RHS according to the MRs) failed. Erroneously, the analog designer has chosen to use *Taylor Series Expansion* in the approximation algorithm of *I_LNA* for the non-linearity region and did not consider the occurrence of higher-order polynomials [4]. This bug was discussed with our industrial cooperation partner and they decided to fix the model accordingly using the concepts from [15]. We received a fixed model which is denoted *I_LNA-fixed*. An excerpt of *I_LNA-fixed* is shown in Fig. 4. Now, in *I_LNA-fixed* no further bugs have been found with our MT-based verification approach.

In the next section we analyze the general quality of our approach in detecting bugs.

5.3 Fault-Detection Quality of MT-based Verification

To show the general quality of our MT-approach in detecting faults without the need of a reference model, we perform a fault-injection campaign on the fixed *I_LNA-fixed* as the second set of experiments. The high-level idea is to inject faults in *I_LNA-fixed* to create *mutants* (faulty versions of *I_LNA-fixed*). Then, for these mutants (a) the shipped test-stimuli are executed and (b) our MT-approach is employed.

The fault-injection campaign requires high quality mutants which mimic potential faults. To this end, we injected several faults in to

```
1    ...
2    void lna_base_pb::processing() {
3    double out_temp;
4    if(p.use_iip3_cp1)
5    out_temp = s.a*p_in - s.b*pow(p_in,2.0) - s.c_ip3*pow(p_in,3.0);
6    else
7    out_temp = s.a*p_in - s.b*pow(p_in,2.0) - s.c_icp*pow(p_in,3.0);
8
9    double vlim=0.0;
10   // clipping
11   if(p_in < s.in_max && p_in > s.in_min)
12   vlim = out_temp;
13   else if(p_in >0.0)
14   vlim = s.a*s.in_max - s.b*pow(s.in_max,2.0) - s.c_ip3*pow(s.in_max,3.0);
15   else
16   vlim = s.a*s.in_min - s.b*pow(s.in_min,2.0) - s.c_ip3*pow(s.in_min,3.0);
17
18   // write outport and signals
19   p_out.write(vlim);
20   }
21   ....
```

Figure 4: Excerpt of SystemC-AMS LNA behavior model

the *I_LNA-fixed* SystemC-AMS model. Since, the LNA system-level model is in principle a C++ code, therefore, as a fault model we target common modeling mistakes in the functionality of C++ [1]. The mutants are automatically generated by an *in-house* tool implemented using the *LibTooling* library for *Clang* compiler.

The tool generated a total of 175 mutants for the *I_LNA-fixed* model. Our proposed MT-based verification approach detected all the 175 mutants, whereas the shipped test-stimuli missed 52 mutants. Results of only 5 test-cases for the experiments are shown in Fig. 5 for visual clarity. The *x-axis* shows the developed MRs and the *y-axis* shows the detected mutants by each MR. The total time it took to simulate one test-case and 175 mutants was approximately 13 minutes. This time includes compilation, base test-stimuli execution, and follow-up test-stimuli execution. All MRs managed to detect at least one fault, which indicates the different fault-detection quality of the MT-based verification. We now discuss one concrete *faulty LNA* (FLNA) to show the effectiveness how MRs detected the fault:

FLNA: Consider a mutation where we negate the condition in Line 4 of Fig. 4, i.e. *if(!p.use_iip3_cp1)*. This injected fault makes the LNA a linear device, hence, it never saturates. When the given test-stimuli are used as input, the LNA behaves linearly as expected and the fault is not detected. The corresponding *Gain (dB)* and *output power (dBm)* curves of the LNA are shown in Fig. 6 and Fig. 7, respectively. They have input power (dBm) on the *x-axis* and gain/output power on the *y-axis*. Different color/marker curves represent different frequencies. Simply put, the injected bug cannot be detected using the given test-stimuli.

However, the MT-based verification approach can detect the fault using both the given test-stimuli and the follow-up test-stimuli. The *relation check* verifies the DUV correctness by comparing the sides of MRs. In this case, out of 12 MRs, only **MR**6 and **MR**7 were able to detect the faulty behavior. Consider **MR**7 which looks at the saturation of the LNA, it states that at high input power, i.e., power corresponding to 2 V (33 dBm) and above, the DUV gain should decrease such that the gain at the follow-up test-case should be lower than the base test-case. When we apply a follow-up test-case with input signal power of 36 dBm, we observe that MR7 fails. The corresponding behavior can be seen in Fig. 6 where the *actual gain* of the LNA stays constant (blue lines). The LNA never saturates and passes all the given test-stimuli, but fails the **MR**7. Similarly, **MR**6 looks at output power of the LNA corresponding to very high input

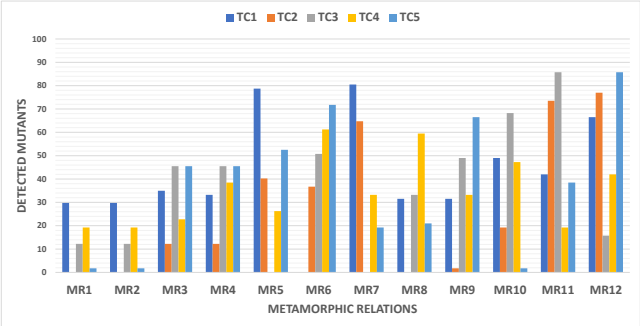


Figure 5: Fault-Detection quality of MT-based verification

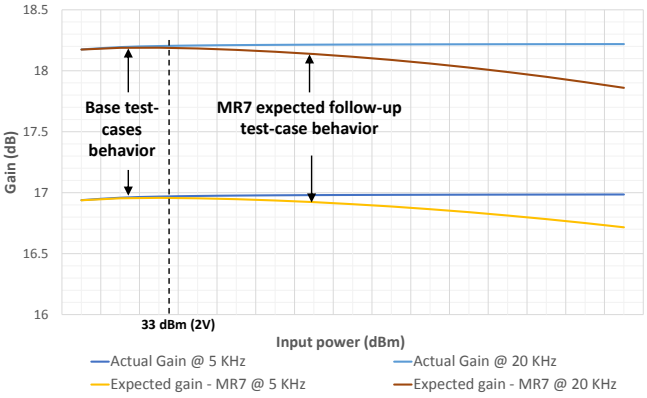


Figure 6: Gain Output of FLNA

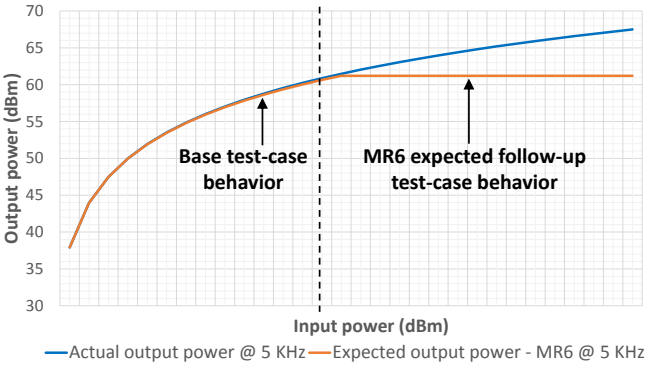


Figure 7: Power Output of FLNA

power. The base test-cases pass and still the fault is not detected during the given test-stimuli execution. However, **MR**6 is able to detect it using the follow-up test-case, as shown in Fig. 7. **MR**6 looks at the output power of the amplifier in saturation and expects that it should remain constant when base test-case and follow-up test-case are applied. However, the actual output power (blue line) as shown in Fig. 7 keeps on increasing as the input power increases, hence, **MR**6 fails.

To summarize the experiments, the MT-based approach effectively verifies the linear and non-linear behavior of the RF amplifiers without the need of reference models.

6 CONCLUSION

In this paper, we have introduced a novel MT-approach for the verification of linear and non-linear behaviors of RF amplifiers at the system-level. We leveraged the MT principles and identified a set of 12 high-quality MRs. In an extensive set of experiments on an industrial system-level LNA model, we have demonstrated the ability to find non-trivial bugs without the need of reference models.

For future work, we plan to investigate the following directions: 1) validate the MT-approach at SPICE-level, 2) apply the MT-approach to other classes of AMS designs. Another very interesting research direction is to devise solutions for determining the completeness of a set of MRs.

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