South European Test Seminar 2018

Program

Monday, February 19

Opening Session

Monday	
Slot 1	Welcome Introduction

Tuesday, February 20

Morning Session *Faster-than-at-Speed-Test*

Tuesday	Speaker	Title of talk
Slot 1	Matthias Kampmann (Paderborn University)	Scan Configuration for FAST considering Fault Information
Slot 2	Alexander Sprenger (Paderborn University)	Tuning Stochastic Space Compaction to Faster-than-at-Speed-Test
Slot 3	Mohammad Maaz (Paderborn University)	Towards an Optimal Space Compactor for FAST

Afternoon Session *Low-Power, AMS & Defect-Oriented Test*

Tuesday	Speaker	Title of talk
Slot 1	Harshad Dhotre (University of Bremen)	Test Pattern Analysis for Localizing Power Activity
Slot 2	Tobias Paxian (University of Freiburg)	About Optimizing Sorting Networks with Cascadic Structure
Slot 3	Felix Neubauer (University of Freiburg)	Efficient Generation of Parametric Test Vectors for AMS Chips with an Interval Constraint Solver
Slot 4	Zahra Paria Najafi Haghi (University of Stuttgart)	Variation Effect on Small Delay Fault Detection

Wednesday, February 21

Morning Session *Design Security*

Wednesday	Speaker	Title of talk
Slot 1	Mael Gay (University of Stuttgart)	Detection of Malicious and Correction of Natural Faults in Cryptographic Circuits
Slot 2	Dennis Gnad (KIT)	Security Threats from Sharing FPGA Fabric
Slot 3	Emanuele Valea (LIRMM)	Test Standards and Security

Morning Session *Online Fault Diagnosis & Self-Verification*

Wednesday	Speaker	Title of talk
Slot 1	Safa Mhamdi (LIRMM)	Systems-on-Chip Diagnosis for Automotive Applications
Slot 2	Buse Ustaoglu (DFKI GmbH)	SAT-Lancer: A Hardware SAT-Solver for Self-Verification

Afternoon Session

Wednesday	
Slot 1	Social Event

Thursday, February 22

Morning Session *Design for Reliability & Fault Tolerance*

Thursday	Speaker	Title of talk
Slot 1	Bastien Deveautour (LIRMM)	Exploring Advantages of Approximate Computing in Logic Hardening
Slot 2	Frank Sill Torres (UFMG)	Sensor-based Detection of Radiation-induced Transient Single-Event Effects
Slot 3	Davide Piumatti (Politecnico di Torino)	Identifying functionally untestable faults in microprocessor cores for safety-critical applications

Afternoon Session *Security in Test & Scan Architecture*

Thursday	Speaker	Title of talk
Slot 1	Natalia Kaptsova (University of Stuttgart)	Security Quantification for On-Chip Infrastructure
Slot 2	Ahmed Atteya (University of Stuttgart)	Online Prevention of Security Violations in Reconfigurable Scan Networks
Slot 3	Pascal Raiola (University of Freiburg)	Design of Reconfigurable Scan Networks for Secure Data Transmission
Slot 4	Rehab Massoud (University of Bremen)	Time-stamps for Hardware Simulation Models Accurate Time-back Annotation

Friday, February 23

Closing Activities

Friday	February 23
Slot 1	Closing Session