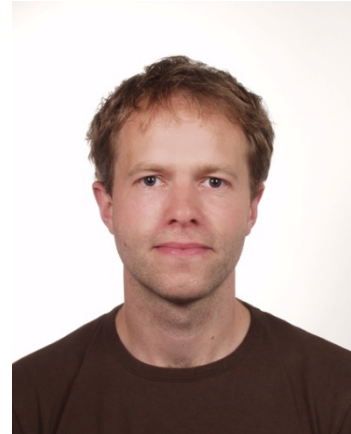

Curriculum Vitae

Dr.-Ing. Görschwin Fey

Gender: Male
Nationality: German
Year of Birth: 1975



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Education

- 2002-2006 Universität Bremen, Germany
Dr.-Ing. (summa cum laude), Advisor: Prof. Dr. Rolf Drechsler
Thesis: Increasing Robustness and Usability of Circuit Design Tools
Using Formal Techniques
- 1995-2001 Martin-Luther-Universität Halle-Wittenberg, Halle (Saale), Germany
Diploma in Computer Science, Advisor: Prof. Dr. Paul Molitor
- 1998-1999 Trinity College, Dublin, Ireland
Student of Computer Science
- 1991-1994 Modellschule Obersberg, Bad Hersfeld, Germany
General university entry levels

Work

- Since 2010 Universität Bremen, Germany
Leader of a junior research group and post-doc (permanent position)
within the group of Prof. Dr. Rolf Drechsler
- 2007-2008 University of Tokyo, Japan
Guest Associate Professor
- 2007 University of Toronto, Canada
Visiting researcher (july/august, 2 weeks)
- 2006-2010 Universität Bremen, Germany
Post-doc (permanent position), group of Prof. Dr. Rolf Drechsler
- 2005 University of Pisa, Italy
Visiting Researcher (november, 2 weeks)
- 2005 Siemens AG, Munich
Visiting researcher, Verification of communication IP block, 2 months
- 2004 University of Massachusetts at Amherst, USA
Visiting researcher (may, 2 weeks)
- 2003 University of Massachusetts at Amherst, USA
Visiting researcher (march, 2 weeks)
- 2002 Siemens AG, Munich
Visiting researcher, Verification of UMTS IP block, 3 months
- 2002-2006 Universität Bremen, Germany
Researcher and teaching assistant, Group of Prof. Dr. Rolf Drechsler
- 1994-1995 Ev. Church, Johannesberg, Bad Hersfeld, Germany
Civil Service

Research Interests

- Formal Verification of Hardware
- Abstract Description Languages
- Automatic Test Pattern Generation
- Diagnosis and Debugging
- Robustness Checking
- Highly Automated Design Tools

Project Experience

Primary investigator

- 2010-2012 DSy – Debugging Eingebetteter Systeme (Debugging of Embedded Systems)
- Research project funded by the German Research Foundation (DFG) within the Emmy Noether Programme
- 2010-2012 Diagnosis, Error Modelling and Correction for Reliable Systems Design (DIAMOND)
- Collaborative research project project funded by the European Union (EU) within the 7th framework programme
 - Co-investigator with Prof. Dr. Rolf Drechsler
- 2009-2011 Design Methodology for Embedded Systems
- Exchange project funded by DAAD (German Academic Exchange Service)
 - Cooperation with Prof. Dr. Masahiro Fujita and Prof. Dr. Satoshi Komatsu, University of Tokyo, Japan
- 2009-2010 Erreichbarkeitsanalyse unter Verwendung von Wortebenen-Beweisern (Reachability Analysis using Word Level Provers)
- Exchange project funded by DAAD
 - Cooperation with Prof. Dr. Andreas Veneris, University of Toronto, Canada
- Since 2008 Formaler Robustheitsnachweis (Formal Robustness Checking)
- Research project funded by DFG
 - Co-investigator with Prof. Dr. Rolf Drechsler

Organization and Participation

- 2007-2010 Verisoft-XT
- Funded by BMBF (Federal Ministry for Education and Research)
 - 17 academic and industrial partners
 - Cooperation with Dr. Michael Siegel, OneSpin Solutions GmbH
- 2006-2009 Herkules: Hardware Entwurfstechnik für Null-Fehler Designs (Hardware Design Methodology for Zero-Fault Designs)
- Research project funded by BMBF
 - Subcontractor of Concept Engineering GmbH, Freiburg, Germany
 - Cooperation with Gerhard Angst and Lothar Linhard
- 2006-2008 Hierarchische und sequentielle Informationen für Erfüllbarkeitsbeweise im Computergestützten Schaltkreisentwurf (Hierarchical and sequential Information for Proofs of Satisfiability in Computer Aided Design of Circuits)
- Exchange project funded by DAAD
 - Cooperation with Prof. Dr. Andreas Veneris, University of Toronto, Toronto, Canada
- 2006-2008 MAYA: Neue Methoden für den Massiv-Parallel-Test im Hochvolumen, Yield Learning und beste Testqualität (New Methods for Massively Parallel Testing in High Volume, Yield Learning and Best Test Quality)
- Research project funded by BMBF
 - Subcontractor of NXP Semiconductors Germany GmbH, Hamburg, Germany
 - Cooperation with Friedrich Hapke

- 2005-2006 Testsynthese von Schaltungen geringer Laufzeit
(Test Synthesis of Circuits with Small Delay)
- Exchange project funded by DAAD
 - Cooperation with Prof. Dr. Anna Bernasconi, Universita di Pisa, Pisa, Italy
- 2005 Industrial verification project (2 months)
- Funded by Siemens AG, München, Germany
 - Verification of communication IP block

Participation

- 2003-2005 Schaltungs- und Systemverifikation auf der Wortebene
(Verification of Circuits and Systems on the Word Level)
- Exchange project funded by DAAD
 - Cooperation with Prof. Dr. Maciej Ciesielski, University of Massachusetts, Amherst, USA
- 2002-2004 VALSE-XT: Eine integrierte Lösung für die SoC-Verifikation
(An Integrated Solution for SoC-Verification)
- Research project funded by BMBF
 - Subcontractor of Infineon Technologies AG, Munich, Germany
 - Cooperation with Prof. Dr. Wolfram Büttner
- 2002 Industrial verification project (3 months)
- Funded by Siemens AG, München, Germany
 - Verification of UMTS IP block

Teaching

Lecture at the University of Tokyo (English)

- Testing of Digital Circuits (summer '08)
- **Lectures at Universität Bremen (German)**
- Qualitätsorientierter Hardware-Entwurf (summer '07, summer '09, summer'10)
- Rechnerarchitektur (winter '06)
- Hardware-Software Co-Design (winter '09)
- Technische Informatik 1 (summer '09)
- Test von Schaltungen und Systemen (winter '08)

Seminars at Universität Bremen (German)

- Methoden der Verifikation (summer '05, winter '05, '06)
- Moderne Aspekte der Rechnerarchitektur (summer '04, '05, '09, winter '04)
- Test Digitaler Schaltungen (summer '04, '05, winter '05)

Student team projects (duration 2 years) at Universität Bremen

- McChip – Multi-Core Chip (winter'10-summer'12)
- YMo – Your Mobile (winter '08-summer '10)
- SPEED – Spezifikation und Dokumentation von Systemen (winter '06-summer '08)
- SATRIX – Algorithmen für Boolesche Erfüllbarkeit (winter '04-summer '06)
- FunTaskIC – Eine integrierte Entwurfsumgebung für SystemC (winter '02-summer '04)

Advised diploma theses at Universität Bremen

- Philipp Klaffert, Fehlertolerante Schaltkreise mit geringem Ressourcenbedarf unter Verwendung partieller Redundanz, 2010
- Jan Carstens, Testmustergenerierung durch Kombination Boolescher Beweiser, 2009

- Stefan Frehse, Formaler Nachweis der Fehlertoleranz von Schaltungen, 2008
Informally advised diploma theses at Universität Bremen
- Marc Messing, Evaluierung neuer Ansätze zur Fehlersortierung bei der automatischen Testmuster-generierung, 2008
- Tim Cassens, Statische Kompaktierung von Testmustern für Schaltkreise, 2007
- Marcin Grden, Überdeckungsmaße in der formalen Hardware Verifikation, 2006
- Tim Warode, Strukturelles Lernen in der erfüllbarkeitsbasierten Testmuster-generierung, 2006
- Michael Klemm, Testmusterkompaktierung mit Genetischen Algorithmen, 2006
- Robert Wille, Erstellung von Free Binary Decision Diagrams mit SAT-Beweisern, 2006
- Stephan Eggersgluß, Testmuster-generierung für Pfadverzögerungsfehler für industrielle Schaltkreise auf Basis des Erfüllbarkeitsproblems, 2006
- Sebastian Kinder, Speichereffiziente Manipulation von Entscheidungsdiagrammen: Theorie und Implementierung, 2005

Awards

2010	Acceptance for Emmy Noether Programme by DFG
2010	Best Paper Award, IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems, Vienna, Austria
2007	Nomination for the German Society of Computer Science (GI) Award for Best Dissertation 2006
2006	Best Paper Award, Haifa Verification Conference, Haifa, Israel
2001	Award for the diploma thesis by CANTOR Unternehmensberatung GmbH, Halle, Germany

Reviewer Activity

Institutions	ARTEMIS Joint Undertaking, European Commission, 2009, 2010
Journals	IEEE Transactions on Computer Aided Design, IEEE Press IEEE Transactions on VLSI, IEEE Press IET Computers & Digital Techniques, IEE IT Information Technology, Oldenbourg Wissenschaftsverlag Journal of Applied Logic, Elsevier Journal on Satisfiability, Boolean Modeling and Computation, IOS Press, Delft University Microprocessors and Microsystems, Elsevier Theory of Computing Systems, Springer
Conferences (excerpt)	Design Automation and Test in Europe (DATE), 2006-2009 Design Automation Conference (DAC), 2009-2011 Euromicro Conference on Digital System Design (DSD), 2007-2011 Forum on Design Languages (FDL), 2007 International Conference on Computer Aided Design (ICCAD), 2007, 2009, 2010 International Symposium on Multiple-Valued Logic (ISMVL), 2007, 2009 International Test Conference (ITC), 2010 Midwest Symposium on Circuits and Systems, 2008, 2009 and other conferences related to circuit design

Work in Academic Bodies

2011	IEEE European Test Symposium (ETS), Program committee member
2011	Student forum at the Asia and South Pacific Design Automation Conference (ASP-DAC), Program committee member
2010	Special session on "Design closure for reliability" at the Design Automation Conference (DAC), Organizer
2009-2011	"GI/GMM/ITG 21. Workshop für Testmethoden und Zuverlässigkeit von Schaltungen und Systemen", Program committee member
2009-2011	Special Session on Fault Tolerance in Digital Systems Design at the Euromicro Conference on Digital System Design (DSD), Program committee member
2009-2011	"GMM/GI/ITG-Fachtagung Fachtagung Zuverlässigkeit und Entwurf", Program committee member
2009	International Workshop on Constraints in Formal Verification (CFV), Program committee member
Since 2007	GI Section 4 "Beschreibungssprachen und Modellierung von Schaltungen und Systemen (RSS-Modell)" of "Kooperationsgemeinschaft Rechnergestützter Schaltungs- und Systementwurf (RSS)", Administration member
Since 2007	Budget Committee Faculty 3, Universität Bremen
2005-2007	Faculty Council, Faculty 3, Universität Bremen

Memberships

- IEEE, GI (German Society of Computer Science)

Publications

- See attachment

References

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Bremen, June 03, 2011