
Dr.-Ing. Görschwin Fey – Publications

Diploma Thesis

- [1] G. Fey. *Set partitioning in hierarchical trees: eine FPGA-Implementierung*. Diploma thesis, Martin Luther Universität, Halle-Wittenberg, Germany, Oct 2001.

Dissertation

- [1] G. Fey. *Increasing Robustness and Usability of Circuit Design Tools by Using Formal Techniques*. Dissertation, Universität Bremen, Bremen, Germany, Dec 2006.

Patent

- [1] G. Fey, Y. Furukawa, S. Komatsu, and M. Fujita. Targeting leakage constraints during ATPG. Pending (submitted to US patent office), 2008.

Books

- [1] R. Drechsler, S. Eggersglüß, G. Fey, and D. Tille. *Test Pattern Generation using Boolean Proof Engines*. Springer, 2009. to appear.
- [2] G. Fey and R. Drechsler. *Robustness and Usability in Modern Design Flows*. Springer, 2008.
- [3] R. Ebdendt, G. Fey, and R. Drechsler. *Advanced BDD Optimization*. Springer, 2005.

Edited Books

- [1] D. Große, G. Fey, and R. Drechsler, editors. *SATRIX – Algorithmen für Boolesche Erfüllbarkeit*. Shaker Verlag, 2007.
- [2] G. Fey and R. Drechsler, editors. *FunTaskIC - Eine integrierte Entwurfsumgebung für SystemC*. Shaker Verlag, 2005.

Bookchapters

- [1] G. Fey. Increasing robustness and usability of circuit design tools by using formal techniques. In D. Wagner et al., editor, *Ausgezeichnete Informatikdissertationen 2006*, volume D-7 of *LNI*, pages 29–38. Gesellschaft für Informatik, 2007.
- [2] R. Drechsler and G. Fey. Automatic test pattern generation. In M. Bernardo and A. Cimatti, editors, *School on Formal Methods for Hardware Verification*, volume 3965 of *LNCS*, pages 30–55. Springer, 2006.

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