
Dr.-Ing. Görschwin Fey – Publications

Diploma Thesis

- [1] G. Fey. *Set partitioning in hierarchical trees: eine FPGA-Implementierung*. Diploma thesis, Martin Luther Universität, Halle-Wittenberg, Germany, Oct 2001.

Dissertation

- [1] G. Fey. *Increasing Robustness and Usability of Circuit Design Tools by Using Formal Techniques*. Dissertation, Universität Bremen, Bremen, Germany, Dec 2006.

Patents and Patent Applications

- [1] Y. Furukawa, G. Fey, S. Komatsu, and M. Fujita. Test apparatus, test method, program, and recording medium reducing the influence of variations. United States patent application no. 20100114520 (pending), 2008.
- [2] Y. Furukawa, G. Fey, S. Komatsu, and M. Fujita. Test apparatus, test vector generate unit, test method, program, and recording medium. United States patent no. US 7,984,353 B2, 2011.

Books

- [1] R. Drechsler, S. Eggersglüß, G. Fey, and D. Tille. *Test Pattern Generation using Boolean Proof Engines*. Springer, 2009.
- [2] G. Fey and R. Drechsler. *Robustness and Usability in Modern Design Flows*. Springer, 2008.
- [3] R. Ebdendt, G. Fey, and R. Drechsler. *Advanced BDD Optimization*. Springer, 2005.

Edited Books

- [1] D. Große, G. Fey, and R. Drechsler, editors. *SATRIX – Algorithmen für Boolesche Erfüllbarkeit*. Shaker Verlag, 2007.
- [2] G. Fey and R. Drechsler, editors. *FunTaskIC - Eine integrierte Entwurfsumgebung für SystemC*. Shaker Verlag, 2005.

Bookchapters

- [1] G. Fey. Assessing system vulnerability using formal verification techniques. In *Annual Doctoral Workshop on Mathematical and Engineering Methods in Computer Science (MEMICS)*, volume 7119 of LNCS, pages 47–56, 2011.
- [2] D. Große, G. Fey, and R. Drechsler. Enhanced formal verification flow for circuits integrating debugging. In R. Ubar, J. Raik, and H. T. Vierhaus, editors, *Design and Test Technology for Dependable Systems-on-Chip*, pages 119–129. IGI Global, 2011.
- [3] R. Wille, G. Fey, D. Große, S. Eggersglüß, and R. Drechsler. SWORD: A SAT like prover using word level information. In *VLSI-SoC: Advanced Topics on Systems on a Chip*, volume 291 of IFIP Advances in Information and Communication Technology, pages 175–192. Springer, 2009. Extended versions of best papers from VLSI-SoC 2007.
- [4] G. Fey. Increasing robustness and usability of circuit design tools by using formal techniques. In D. Wagner et al., editor, *Ausgezeichnete Informatikdissertationen 2006*, volume D-7 of LNI, pages 29–38. Gesellschaft für Informatik, 2007.
- [5] R. Drechsler and G. Fey. Automatic test pattern generation. In M. Bernardo and A. Cimatti, editors, *School on Formal Methods for Hardware Verification*, volume 3965 of LNCS, pages 30–55. Springer, 2006.

Journals

- [1] G. Fey, A. Süllow, S. Frehse, and R. Drechsler. Effective robustness analysis using bounded model checking techniques. *IEEE Transactions on Computer Aided Design of Circuits and Systems (TCAD)*, 30(8):1239–1252, 2011.
 - [2] G. Fey, A. Süllow, S. Frehse, and R. Drechsler. Automatische formale Verifikation der Fehlertoleranz von Schaltkreisen. *it – Information Technology*, 52(4):216–222, 2010.
 - [3] S. Eggersglüß, G. Fey, A. Glowatz, F. Hapke, J. Schloeffel, and R. Drechsler. MONSOON: SAT-based ATPG for path delay faults using multiple-valued logics. *Journal of Electronic Testing: Theory and Applications (JETTA)*, 26(3):307–322, 2010.
-

- [4] F. Rogin, T. Klotz, G. Fey, R. Drechsler, and S. Rülke. Advanced verification by automatic property generation. *IET Computers and Digital Techniques*, 3(4):338–353, 2009.
- [5] R. Drechsler, S. Eggersglüß, G. Fey, and D. Tille. Effiziente Erfüllbarkeitsalgorithmen für die Generierung von Testmustern. *it – Information Technology*, 51(2):102–111, 2009.
- [6] R. Drechsler, S. Eggersglüß, G. Fey, A. Glowatz, F. Hapke, J. Schlöffel, and D. Tille. On acceleration of SAT-based ATPG for industrial designs. *IEEE Transactions on Computer Aided Design of Circuits and Systems (TCAD)*, 27(7):1329–1333, 2008.
- [7] G. Fey, A. Bernasconi, V. Ciriani, and R. Drechsler. On the construction of small fully testable circuits with low depth. *Microprocessors and Microsystems (MICPRO)*, 32(5-6):263–269, 2008.
- [8] G. Fey, S. Staber, R. Bloem, and R. Drechsler. Automatic fault localization for property checking. *IEEE Transactions on Computer Aided Design of Circuits and Systems (TCAD)*, 27(6):1138–1149, 2008.
- [9] R. Wille, G. Fey, and R. Drechsler. Building free binary decision diagrams using SAT solvers. *Facta Universitatis*, 20(3):381–394, December 2007.
- [10] R. Drechsler, G. Fey, and S. Kinder. An integrated approach for combining BDDs and SAT provers. *Facta Universitatis*, 20(3):415–436, December 2007.
- [11] G. Fey and R. Drechsler. Minimizing the number of paths in BDDs - theory and algorithm. *IEEE Transactions on Computer Aided Design of Circuits and Systems (TCAD)*, 25(1):4–11, 2006.
- [12] A. Breiter, G. Fey, and R. Drechsler. Project-based learning in student teams in computer science education. *Facta Universitatis*, 18(2):165–180, August 2005.
- [13] R. Drechsler, J. Shi, and G. Fey. Synthesis of fully testable circuits from BDDs. *IEEE Transactions on Computer Aided Design of Circuits and Systems (TCAD)*, 23(3):440–443, 2004.

Conferences

- [1] M. Dehbashi and G. Fey. Automated post-silicon debugging of design bugs. In *System, Software, SoC and Silicon Debug Conference (S4D)*, pages 67–71, 2011.
- [2] S. Frehse, F. Haedicke, M. Diepenbeck, G. Fey, and R. Drechsler. Hochoptimierter Ablauf zur Robustheitsprüfung. In *GMM/GI/ITG-Fachtagung Zuverlässigkeit und Entwurf (ZUE)*, pages 35–42, 2011.
- [3] M. Dehbashi, A. Sülflow, and G. Fey. Automated design debugging in a testbench-based verification environment. In *EUROMICRO Symposium on Digital System Design (DSD)*, pages 479–486, 2011.
- [4] G. Fey. Orchestrated multi-level information flow analysis to understand SoCs. In *Design Automation Conference (DAC)*, pages 284–285, 2011.
- [5] M. Soeken, U. Kühne, M. Freibothe, G. Fey, and R. Drechsler. Towards automatic property generation for the formal verification of bus bridges. In *IEEE Int'l Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS)*, pages 417–422, 2011.
- [6] A. Finder, A. Sülflow, and G. Fey. Latency analysis for sequential circuits. In *IEEE European Test Symposium (ETS)*, pages 129–134, 2011.
- [7] F. Haedicke, B. Alizadeh, G. Fey, M. Fujita, and R. Drechsler. Polynomial datapath optimization using constraint solving and formal modelling. In *IEEE/ACM Int'l Conf. on CAD (ICCAD)*, pages 756–761, 2010.
- [8] A. Finder and G. Fey. Evaluating debugging algorithms from a qualitative perspective. In *Forum on Specification and Design Languages (FDL)*, 2010.
- [9] S. Frehse and G. Fey. Kompositionelle Formale Robustheitsprüfung. In *GMM/GI/ITG-Fachtagung Zuverlässigkeit und Entwurf (ZUE)*, pages 73–74, 2010.
- [10] S. Frehse, G. Fey, A. Sülflow, and R. Drechsler. RobuCheck: A robustness checker for digital circuits. In *EUROMICRO Symposium on Digital System Design (DSD)*, pages 226–231, 2010.
- [11] A. Sülflow, G. Fey, and R. Drechsler. Using QBF to increase accuracy of SAT-based debugging. In *IEEE Int'l Symposium on Circuits and Systems (ISCAS)*, pages 641–644, 2010.
- [12] S. Frehse, G. Fey, and R. Drechsler. A better-than-worst-case robustness measure. In *IEEE Int'l Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS)*, pages 78–83, 2010. Best paper award.

- [13] G. Fey. Deterministic algorithms for ATPG under leakage constraints. In *Asian Test Symposium (ATS)*, pages 313–316, 2009.
- [14] G. Fey, A. Sülflow, and R. Drechsler. Computing bounds for fault tolerance using formal techniques. In *Design Automation Conference (DAC)*, pages 190–195, 2009.
- [15] T. Nakura, Y. Tatemura, G. Fey, M. Ikeda, S. Komatsu, and K. Asada. SAT-based ATPG testing of inter- and intra-gate bridging faults. In *European Conference on Circuit Theory and Design (ECCTD)*, pages 643–647, 2009.
- [16] S. Frehse, G. Fey, A. Sülflow, and R. Drechsler. Robustness check for multiple faults using formal techniques. In *EUROMICRO Symposium on Digital System Design (DSD)*, pages 85–90, 2009.
- [17] A. Sülflow, S. Frehse, G. Fey, and R. Drechsler. Anwendungsbezogene Analyse der Robustheit von digitalen Schaltungen. In *GMM/GI/ITG-Fachtagung Zuverlässigkeit und Entwurf (ZUE)*, pages 45–52, 2009.
- [18] A. Sülflow, U. Kühne, G. Fey, D. Große, and R. Drechsler. WoLFram – a word level framework for formal verification. In *IEEE/IFIP Int'l Symposium on Rapid System Prototyping (RSP)*, pages 11–17, 2009.
- [19] A. Sülflow, R. Wille, G. Fey, and R. Drechsler. Evaluation of cardinality constraints on SMT-based debugging. In *IEEE Int'l Symposium on Multi-Valued Logic (ISMVL)*, pages 298–303, 2009.
- [20] A. Sülflow, G. Fey, C. Braunstein, U. Kühne, and R. Drechsler. Increasing the accuracy of SAT-based debugging. In *Design, Automation and Test in Europe (DATE)*, pages 1326–1331, 2009.
- [21] G. Fey, S. Komatsu, Y. Furukawa, and M. Fujita. Targeting leakage constraints during ATPG. In *Asian Test Symposium (ATS)*, pages 225–230, 2008.
- [22] G. Fey, A. Sülflow, S. Frehse, U. Kühne, and R. Drechsler. Formaler Nachweis der Fehlertoleranz von Schaltkreisen. In *GMM/GI/ITG-Fachtagung Zuverlässigkeit und Entwurf (ZUE)*, pages 75–82, 2008.
- [23] R. Wille, G. Fey, M. Messing, G. Angst, L. Linhard, and R. Drechsler. Identifying a subset of System Verilog assertions for efficient bounded model checking. In *EUROMICRO Symposium on Digital System Design (DSD)*, pages 542–549, 2008.
- [24] F. Rogin, T. Klotz, G. Fey, R. Drechsler, and S. Rülke. Automatic generation of complex properties for hardware designs. In *Design, Automation and Test in Europe (DATE)*, pages 545–548, 2008.
- [25] A. Sülflow, G. Fey, R. Bloem, and R. Drechsler. Using unsatisfiable cores to debug multiple design errors. In *Great Lakes Symp. VLSI (GLS)*, pages 77–82, 2008.
- [26] G. Fey and R. Drechsler. A basis for formal robustness checking. In *Int'l Symposium on Quality Electronic Design (ISQED)*, pages 784–789, 2008.
- [27] R. Wille, G. Fey, D. Große, S. Eggersglüß, and R. Drechsler. SWORD: A SAT like prover using word level information. In *IEEE/IFIP Int'l Conference on VLSI and System-on-Chip (VLSI-SoC)*, pages 88–93, 2007.
- [28] G. Fey, A. Bernasconi, V. Ciriani, and R. Drechsler. On the construction of small fully testable circuits with low depth. In *EUROMICRO Symposium on Digital System Design (DSD)*, pages 563–569, 2007.
- [29] S. Eggersglüß, G. Fey, R. Drechsler, A. Glowatz, F. Hapke, and J. Schlöffel. Combining multi-valued logics in SAT-based ATPG for path delay faults. In *ACM/IEEE Int'l Conference on Formal Methods and Models for Codesign (MEMOCODE)*, pages 181–187, 2007.
- [30] S. Eggersglüß, D. Tille, G. Fey, R. Drechsler, A. Glowatz, F. Hapke, and J. Schlöffel. Experimental studies on SAT-based ATPG for gate delay faults. In *IEEE Int'l Symposium on Multi-Valued Logic (ISMVL)*, page 6 (6 pages), 2007.
- [31] G. Fey, T. Warode, and R. Drechsler. Using structural learning techniques in SAT-based ATPG. In *VLSI Design Conference*, pages 69–74, 2007.
- [32] S. Eggersglüß, G. Fey, and R. Drechsler. SAT-based ATPG for path delay faults in sequential circuits. In *IEEE Int'l Symposium on Circuits and Systems (ISCAS)*, pages 3671–3674, 2007.
- [33] G. Fey and R. Drechsler. Ein formaler Ansatz zum Robustheitsnachweis. In *GMM/GI/ITG-Fachtagung Zuverlässigkeit und Entwurf (ZUE)*, pages 101–108, 2007.

- [34] S. Staber, G. Fey, R. Bloem, and R. Drechsler. Automatic fault localization for property checking. In *IBM Haifa Verification Conference (HVC)*, volume 4383 of *LNCS*, pages 50–64. Springer Verlag, 2006. Best paper award.
- [35] G. Fey, J. Shi, and R. Drechsler. Efficiency of multiple-valued encoding in SAT-based ATPG. In *IEEE Int'l Symposium on Multi-Valued Logic (ISMVL)*, page 25 (6 pages), 2006.
- [36] R. Drechsler, G. Fey, and S. Kinder. An integrated approach for combining BDD and SAT provers. In *VLSI Design Conference*, pages 237–242, 2006.
- [37] G. Fey, S. Safarpour, A. Veneris, and R. Drechsler. On the relation between simulation-based and SAT-based diagnosis. In *Design, Automation and Test in Europe (DATE)*, pages 1139–1144, 2006.
- [38] G. Fey, D. Große, and R. Drechsler. Avoiding false negatives in formal verification for protocol-driven blocks. In *Design, Automation and Test in Europe (DATE)*, pages 1225–1226, 2006.
- [39] S. Kinder, G. Fey, and R. Drechsler. Controlling the memory during manipulation of word-level decision diagrams. In *IEEE Int'l Symposium on Multi-Valued Logic (ISMVL)*, pages 250–255, 2005.
- [40] S. Safarpour, G. Fey, A. Veneris, and R. Drechsler. Utilizing don't care states in SAT-based bounded sequential problems. In *Great Lakes Symp. VLSI (GLS)*, pages 264–269, 2005.
- [41] J. Shi, G. Fey, R. Drechsler, A. Glowatz, J. Schlöffel, and F. Hapke. PASSAT: Efficient SAT-based test pattern generation. In *IEEE Annual Symposium on VLSI (ISVLSI)*, pages 212–217, 2005.
- [42] J. Shi, G. Fey, R. Drechsler, A. Glowatz, J. Schlöffel, and F. Hapke. Experimental studies on SAT-based test pattern generation for industrial circuits. In *IEEE Int'l Conference on ASIC (ASICON)*, 2005.
- [43] J. Shi, G. Fey, and R. Drechsler. Bridging fault testability of BDD circuits. In *ASP Design Automation Conference (ASPDAC)*, pages 188–191, 2005.
- [44] G. Fey and R. Drechsler. Improving simulation-based verification by means of formal methods. In *ASP Design Automation Conference (ASPDAC)*, pages 640–643, 2004.
- [45] G. Fey, R. Drechsler, and M. Ciesielski. Algorithms for taylor expansion diagrams. In *IEEE Int'l Symposium on Multi-Valued Logic (ISMVL)*, pages 235–240, 2004.
- [46] K. Winkelmann, H.-J. Trylus, D. Stoffel, and G. Fey. Cost-efficient block verification for a UMTS up-link chip-rate coprocessor. In *Design, Automation and Test in Europe (DATE)*, volume 1, pages 162–167, 2004.
- [47] G. Fey, J. Shi, and R. Drechsler. BDD circuit optimization for path delay fault testability. In *EUROMICRO Symposium on Digital System Design (DSD)*, pages 162–172, 2004.
- [48] R. Drechsler, J. Shi, and G. Fey. MuTaTe: An efficient design for testability technique for multiplexor based circuits. In *Great Lakes Symp. VLSI (GLS)*, pages 80–83, 2003.
- [49] G. Fey and R. Drechsler. Finding good counter-examples to aid design verification. In *ACM/IEEE Int'l Conference on Formal Methods and Models for Codesign (MEMOCODE)*, pages 51–52, 2003.
- [50] G. Fey, S. Kinder, and R. Drechsler. Using games for benchmarking and representing the complete solution space using symbolic techniques. In *IEEE Int'l Symposium on Multi-Valued Logic (ISMVL)*, pages 361–366, 2003.
- [51] D. Große, G. Fey, and R. Drechsler. Modeling multi-valued circuits in SystemC. In *IEEE Int'l Symposium on Multi-Valued Logic (ISMVL)*, pages 281–286, 2003.
- [52] J. Shi, G. Fey, and R. Drechsler. BDD based synthesis of symmetric functions with full path-delay fault testability. In *Asian Test Symposium (ATS)*, pages 290–293, 2003.
- [53] G. Fey and R. Drechsler. Minimizing the number of paths in BDDs. In *Symposium on Integrated Circuits and Systems Design (SBCCI)*, pages 359–364, 2002.
- [54] G. Fey and R. Drechsler. Utilizing BDDs for disjoint SOP minimization. In *IEEE Midwest Symposium on Circuits and Systems (MWSCAS)*, volume 2, pages 306–309, 2002.
- [55] J. Ritter, G. Fey, and P. Molitor. SPIHT implemented in a XC4000 device. In *IEEE Midwest Symposium on Circuits and Systems (MWSCAS)*, volume 1, pages 239–242, 2002.

Workshops

- [1] J. Malburg, A. Finder, and G. Fey. Automated feature localization for hardware designs using coverage metrics. In *ITG/GI/GMM-Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV)*, 2012.
- [2] M. Dehbashi and G. Fey. Automated debugging from pre-silicon to post-silicon. In *GI/GMM/ITG-Workshop für Testmethoden und Zuverlässigkeit von Schaltungen und Systemen (TUZ)*, 2012.
- [3] F. Haedicke, S. Frehse, G. Fey, D. Große, and R. Drechsler. metaSMT: Focus on your application not on solver integration. In *Int'l Workshop on Design and Implementation of Formal Tools and Systems (DIFTS)*, pages 22–29, 2011.
- [4] H. Riener, R. Bloem, and G. Fey. Test case generation from mutants using model checking techniques. In *Mutation*, pages 388–397, 2011.
- [5] A. Finder, A. Sülflow, and G. Fey. Latency analysis for sequential circuits. In *GI/GMM/ITG-Workshop für Testmethoden und Zuverlässigkeit von Schaltungen und Systemen (TUZ)*, pages 119–124, 2011.
- [6] M. Soeken, U. Kühne, M. Freibothe, G. Fey, and R. Drechsler. Towards automatic property generation for the formal verification of bus bridges. In *ITG/GI/GMM-Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV)*, 2011.
- [7] G. Fey, A. Sülflow, and R. Drechsler. Towards unifying localization and explanation for automated debugging. In *International Workshop on Microprocessor Test and Verification (MTV)*, pages 3–8, 2010.
- [8] A. Finder and G. Fey. Evaluating debugging algorithms from a qualitative perspective. In *Int'l Workshop on Boolean Problems (IWSBP)*, 2010.
- [9] S. Frehse, G. Fey, and R. Drechsler. A better-than-worst-case robustness measure. In *GI/GMM/ITG-Workshop für Testmethoden und Zuverlässigkeit von Schaltungen und Systemen (TUZ)*, pages 19–24, 2010.
- [10] S. Frehse, G. Fey, A. Sülflow, and R. Drechsler. RobuCheck: A robustness checker for digital circuits. In *Workshop on Dynamic Aspects in Dependability Model for Fault-Tolerant Systems (DYADEM-FTS)*, pages 37–38, 2010.
- [11] G. Fey. Algorithms for ATPG under leakage constraints. In *GI/GMM/ITG-Workshop für Testmethoden und Zuverlässigkeit von Schaltungen und Systemen (TUZ)*, pages 91–96, 2009.
- [12] S. Frehse, G. Fey, A. Sülflow, and R. Drechsler. Robustness check for multiple faults using formal techniques. In *Workshop on Constraints in Formal Verification (CFV)*, 2009.
- [13] A. Sülflow, G. Fey, and R. Drechsler. Using qbf to increase accuracy of sat-based debugging. In *Workshop on Constraints in Formal Verification (CFV)*, 2009.
- [14] A. Sülflow, G. Fey, C. Braunstein, U. Kühne, and R. Drechsler. Increasing the accuracy of SAT-based debugging. In *ITG/GI/GMM-Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV)*, 2009.
- [15] R. Drechsler, S. Eggersgluß, G. Fey, and D. Tille. SAT-based automatic test pattern generation. In H. Schlingloff, T. E. J. Vos, and J. Wegener, editors, *Evolutionary Test Generation Dagstuhl-Seminar*, number 08351 in Dagstuhl Seminar Proceedings. Schloss Dagstuhl - Leibniz-Zentrum fuer Informatik, Germany, 2009. last access on 2009/06/03.
- [16] A. Sülflow, G. Fey, and R. Drechsler. Experimental studies on SMT-based debugging. In *IEEE Workshop on RTL and High Level Testing (WRTL)*, pages 93–98, 2008.
- [17] A. Sülflow, G. Fey, S. Frehse, U. Kühne, and R. Drechsler. Computing bounds for fault tolerance using formal techniques. In *Workshop on Design for Reliability and Variability (DRV)*, 2008.
- [18] F. Rogin, T. Klotz, S. Rülke, G. Fey, and R. Drechsler. Effiziente automatische Generierung von Assertions für industrielle Hardware-Designs. In *Dresdner Arbeitstagung Schaltungs- und Systementwurf (DASS)*, 2008.
- [19] G. Fey, S. Komatsu, Y. Furukawa, and M. Fujita. Targeting leakage constraints during ATPG. In *IEEE Int'l Workshop on Silicon Debug and Diagnosis (SDD)*, 2008.
- [20] G. Fey and R. Drechsler. Synthesis for detection of transient faults. In *IEICE Workshop on Dependable Computing*, IEICE Technical Report, pages 161–166, 2008. Vol. 107, No. 558.

- [21] A. Sülflow, G. Fey, R. Bloem, and R. Drechsler. Debugging design errors by using unsatisfiable cores. In *ITG/GI/GMM-Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV)*, pages 159–168, 2008.
- [22] G. Fey and R. Drechsler. Formal robustness checking. In *Workshop on Constraints in Formal Verification (CFV)*, 2007.
- [23] S. Kinder, G. Fey, and R. Drechsler. Estimating the quality of AND-EXOR optimization results. In *Int'l Workshop on Applications of the Reed-Muller Expansion in Circuit Design*, 2007.
- [24] R. Wille, G. Fey, and Rolf Drechsler. Building free binary decision diagrams using SAT solvers. In *Int'l Workshop on Applications of the Reed-Muller Expansion in Circuit Design*, 2007.
- [25] D. Tille G. Fey and Rolf Drechsler. Instance generation for SAT-based ATPG. In *IEEE Design and Diagnostics of Electronic Circuits and Systems Workshop (DDECS)*, 2007.
- [26] D. Tille, S. Eggersglüß, Görschwin Fey, R. Drechsler, A. Glowatz, F. Hapke, and J. Schlöffel. Studies on integrating SAT-based ATPG in an industrial environment. In *GI/GMM/ITG-Workshop für Testmethoden und Zuverlässigkeit von Schaltungen und Systemen (TUZ)*, 2007.
- [27] A. Sülflow, G. Fey, and R. Drechsler. Verbesserte SAT basierte Fehlerdiagnose durch Widerspruchsanalyse. In *ITG/GI/GMM-Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV)*, 2007.
- [28] G. Fey, D. Große, S. Eggersglüß, R. Wille, and R. Drechsler. Formal verification on the word level using SAT-like proof techniques. In *ITG/GI/GMM-Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV)*, 2007.
- [29] G. Fey, T. Warode, and R. Drechsler. Using structural learning techniques in SAT-based ATPG. In *Int'l Workshop on Boolean Problems (IWSBP)*, pages 63–69, 2006.
- [30] G. Fey and R. Drechsler. SAT-based calculation of source code coverage for BMC. In *ITG/GI/GMM-Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV)*, pages 163–170, 2006.
- [31] G. Fey, J. Shi, and R. Drechsler. Efficiency of multiple-valued encoding in SAT-based ATPG. In *GI/GMM/ITG-Workshop für Testmethoden und Zuverlässigkeit von Schaltungen und Systemen (TUZ)*, pages 107–108, 2006.
- [32] G. Fey and R. Drechsler. Efficient hierarchical system debugging for property checking. In *IEEE Design and Diagnostics of Electronic Circuits and Systems Workshop (DDECS)*, pages 41–46, 2005.
- [33] R. Drechsler, G. Fey, C. Genz, and D. Große. SyCE: An integrated environment for system design in SystemC. In *IEEE Int'l Workshop on Rapid System Prototyping (RSP)*, pages 258–260, 2005.
- [34] J. Shi, G. Fey, R. Drechsler, A. Glowatz, J. Schlöffel, and F. Hapke. PASSAT: Efficient SAT-based test pattern generation. In *IEEE Design and Diagnostics of Electronic Circuits and Systems Workshop (DDECS)*, pages 166–173, 2005.
- [35] N. Drechsler, M. Hilgemeier, G. Fey, and R. Drechsler. Disjoint sum of product minimization by evolutionary algorithms. In *Applications of Evolutionary Computing: EvoWorkshops*, volume 3005 of *LNCS*, pages 198–207. Springer Verlag, 2004.
- [36] G. Fey and R. Drechsler. Visualization of diagnosis results for design debugging. In *International Workshop on Post-Binary ULSI Systems (ULSIWS)*, pages 1–2, 2004.
- [37] G. Fey, D. Große, T. Cassens, C. Genz, T. Warode, and R. Drechsler. ParSyC: An efficient SystemC parser. In *Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI)*, pages 148–154, 2004.
- [38] G. Fey and R. Drechsler. A hybrid approach combining symbolic and structural techniques for disjoint SOP minimization. In *Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI)*, pages 54–60, 2003.
- [39] G. Fey, J. Shi, and R. Drechsler. BDD circuit optimization for path delay fault-testability. In *GI/GMM/ITG-Workshop für Testmethoden und Zuverlässigkeit von Schaltungen und Systemen (TUZ)*, 2003.
- [40] J. Shi, G. Fey, and R. Drechsler. BDD based synthesis of symmetric functions with full path-delay fault testability. In *IEEE European Test Workshop (ETW)*, pages 109–110, 2003.

- [41] J. Shi, G.Fey, and R. Drechsler. Random pattern testability of circuits derived from BDDs. In *IEEE Workshop on RTL and High Level Testing (WRTL)*, pages 70–78, 2003.
- [42] K. Winkelmann, J. Trylus, D. Stoffel, and G. Fey. Cost-efficient formal block verification for ASIC design. In *ITG/GI/GMM-Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV)*, pages 184–188, 2003.

Tutorials, Special Sessions, and Selected Invited Talks

- [1] G. Fey. Assessing system vulnerability using formal verification techniques. In *Annual Doctoral Workshop on Mathematical and Engineering Methods in Computer Science (MEMICS)*, 2011. Invited talk, published in LNCS 7119, see corresponding reference in bookchapters.
- [2] S. Frehse, G. Fey, and R. Drechsler. A better-than-worst-case robustness measure. In *Int'l Test Conference (ITC)*, 2010. Invited talk on the paper at DDECS'10 in the partner conference track of ITC'10.
- [3] A. Sülflow, G. Fey, and R. Drechsler. Bounded fault tolerance checking. In *Forum on Specification and Design Languages (FDL)*, 2010. Invited talk for a special session.
- [4] G. Fey (organizer). Design closure for reliability. Special Session at Design Automation Conference (DAC), 2010.
- [5] R. Drechsler and G. Fey. Formal verification meets robustness checking – techniques and challenges. Tutorial at IEEE Int'l Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS), 2010.
- [6] R. Drechsler and G. Fey. Formale Verifikation und Robustheit. Tutorial at GMM/GI/ITG-Fachtagung Zuverlässigkeit und Entwurf (ZUE), 2009.
- [7] D. Borrione, R. Drechsler, E. Ecrenez-Tiphene, and G. Fey. Formal and semi-formal methods for correctness and robustness. Organizer of tutorial at Design, Automation and Test in Europe (DATE), 2009.