

Test Scheduling Optimization Model for IEEE 1687 Multi-Power Domain Networks Using Boolean Satisfiability

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Abstract—The IEEE 1687 Std. provides an efficient access methodology for embedded instruments in complex system-on-a-chip designs by introducing reconfigurable scan networks. This flexibility enables the reduction of the overall test access time, which significantly decreases the test costs compared to the conventional daisy-chaining method. However, the new access methodology strictly requires new effective test schedulers that consider multi-power domains with individual constraints, as given on the chip-level. This work proposes a novel SAT-based optimization modeling scheme for complex IEEE 1687 networks with multi-power domains, which yields highly effective but power-safe tests.

I. INTRODUCTION

The steadily increasing number of cores in System-on-a-Chip (SoC) designs has been boosting the demand for highly efficient instrument access methodologies since the last years. The IEEE 1687 Std. [1] – also known as IJTAG – was introduced to integrate reconfigurable scan networks into SoCs. Any on-chip module like a built-in self-test engine that holds a client interface and is accessed/managed by an external controller is referred to as an instrument. The faster instruments' access in IJTAG networks is realized by employing a new component called *Segment Insertion Bit* (SIB), which is programmed to include or exclude the segment of the network that is connected to the host interface on the chip-level. This principle aims at the scan chain's shortening and, hence, the reduction of the access time overhead during test, debug, and monitoring. In every *Capture-Shift-Update* (CSU) cycle, all instruments of the current active chain receive the new data from *scan-in* port and at the same time shift their individual data to *scan-out* port of the chip. Due to the power, temperature, and further system limitations, not all of the SoC's components can be simultaneously tested. Further power demand is introduced when the network components are considered in addition to the instruments' scan and self-test components and, hence, the design is even more prone to issues like IR-drop and test failures [2], [3]. As the overall test time directly affects the test cost, determining an optimized access sequence to the cores massively improves the test procedure and reduces the resulting test costs.

Significant research has been carried out on such an optimization of the test scheduling [4]–[7]. The authors in [5] propose a session-less test scheduling method by sorting the instruments according to their resource conflict and their number of test patterns. In [6], a pre-emptive scheduling

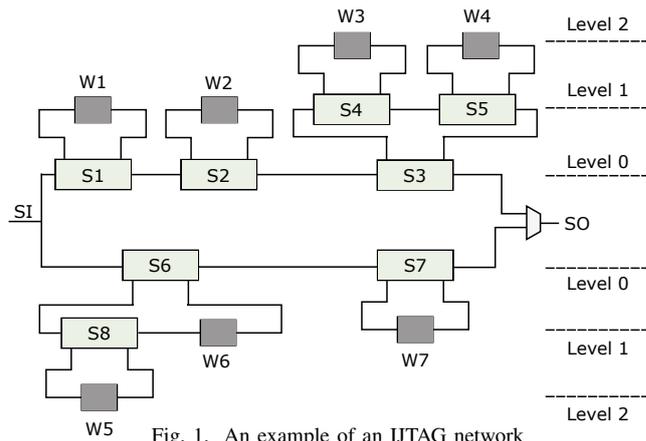


Fig. 1. An example of an IJTAG network

method is introduced, which invokes an exhaustive search over all possible concurrent instruments. The scan architecture of [8] uses a reconfigurable broadcast mechanism to reduce the time required for test data transfer. However, all these works do not consider either any power constraints or do not incorporate multi-power domains, which is strictly required for an effective test of state-of-the-art SoCs. In [7], a graph-based model of IJTAG networks is proposed for the first time, which allows a power-aware test access scheduling in multi-power domain networks. Even if the approach [7] delivers already quite promising results, it typically does not yield an *optimal* solution but remains in local optima. This is since the internal decision-making are, at least, partially done on a greedy-like algorithmic basis.

This work proposes a novel optimization model for the test scheduling in large IJTAG networks with multiple power domains using *Boolean Satisfiability* (SAT). By this, it can be taken advantage of a powerful formal solving engine to, finally, calculate a global optimal test schedule yielding highly effective but power-safe tests.

II. PROPOSED SAT-BASED OPTIMIZATION MODEL

This section presents the proposed model for describing a generic IJTAG network containing *instruments*, *SIBs*, *Scan-Muxes* and branching nodes. This model is then used to obtain an optimal test schedule, which covers all instruments within a minimum overall access time without exceeding the power

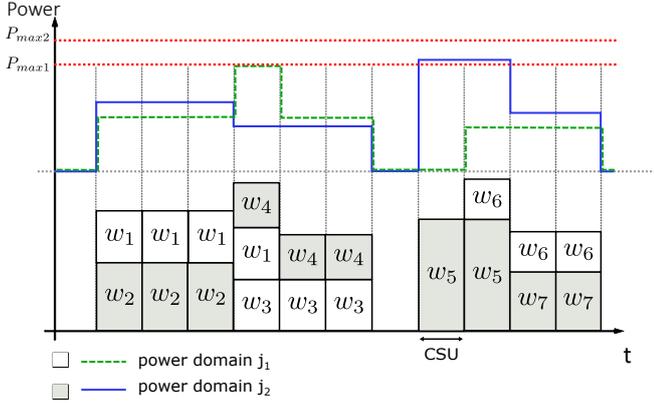


Fig. 3. The scheduling optimization problem

h_2 from the current hierarchy h_1 at least, $h_2 - h_1$ CSUs are required. These criteria yield both a primary Pseudo-Boolean objective function \mathcal{F}_1 and the secondary one \mathcal{F}_2 . \mathcal{F}_1 addresses the minimization of the active hierarchies.

To implement \mathcal{F}_1 , a weight w_i is added to every of the N Boolean variable v_i representing a network component that opens/closes a hierarchical level. The weight is accumulated if the hierarchy is opened, whereby the weight is determined by the actual hierarchical level h_i . \mathcal{F}_1 is defined as follows:

$$\mathcal{F}_1(v_1, \dots, v_N) = \sum_{i=1}^N (w_i \cdot v_i) \quad \text{with} \quad w_i = h_i \quad (5)$$

The second optimization stage (using \mathcal{F}_2) is then applied to reduce the power consumption further, analogously to the enumeration constraints.

D. Incremental Invocation

The blocks of Fig. 3 have to be distributed over the strips such that the minimum number of CSUs is required. This is obtained by allocating the maximum number of instruments within each strip. Since no strip initially exists, 1 is assumed for the SI port's corresponding variable. This yields a path to SO including the maximum number of instruments such that the active instrument does not violate the power limit, as determined by the SAT solver. The set of instruments that have been activated by the SAT solver are considered as the first strip. The next strip is created when the access to at least one of the instruments (of the current set) has been completed. Accordingly, the corresponding literals are assumed as 1 to deactivate the already covered instruments for the solver's next invocation.

III. EVALUATION AND CONCLUSION

For the evaluation of the proposed modeling scheme, a framework has been written in C++, which utilizes the *clasp 3.1.4* Pseudo-Boolean optimization solver [9]. This framework allows for generating a Pseudo-Boolean instance by following the proposed scheme of this work. The networks from the *ITC'16* benchmark set [10] have been considered as a reference.

TABLE I
BENCHMARK IJTAG NETWORKS

benchmark	network	#(nodes,edges)	#instruments	#variables	#clauses
B	Mingle	(27,39)	8	35	62
	BasicSCB	(33,42)	5	39	101
	TreeFlat	(38,61)	11	38	107
C	q12710	(52,78)	23	75	102
	a586710	(94,124)	22	116	303
	t512505	(289,447)	128	417	576
	p22810	(520,789)	242	762	1038
A	N17D3	(52,66)	27	79	144
	N32D6	(79,101)	44	123	216
	N73D14	(155,200)	90	245	426
	N132D4	(293,371)	172	465	825

Table I presents rightmost the number of variables and clauses, which have been obtained while processing the individual ICL network. The benchmark networks have been classified into three groups of complexity, namely basic, classic and advanced. The values – being presented as nodes and edges – represent the total number of elements and their connections in the corresponding graphs. These metrics are meant to provide a general overview of the network scale. The experiments have shown that this model yields Pseudo-Boolean instances, which can be processed in a reasonable run-time.

This paper proposed a novel SAT-based test scheduling optimization model for complex IJTAG test networks with multi-power domains. The proposed model allows determining highly effective but power-safe tests and, by this, contributes to reduced test costs when testing complex and power-critical SoC designs.

IV. ACKNOWLEDGMENT

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