Einladung zum Vortrag

31. Januar 2018, 9 Uhr s.t.
Universität Bremen | MZH 4380
(ACHTUNG | SONDERTERMIN AUSSER DER REIHE)

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SamaTulyata: An Efficient Path Based Equivalence Checker

An application program can go through significant optimizing and parallelizing transformations, both automated and human guided, before being mapped to an architecture. Formal verification of these transformations is crucial to ensure that they preserve the original behavioural specification. Petri net model encompassing data processing is used to model parallel behaviours more vividly. The main objective of the talk is to present a translation validation method for verifying, optimizing and parallelizing code transformations by checking equivalence between two Petri net models, one representing the source code and the other representing its optimized and (or) parallelized version.

Biografie

Dr. Soumyadip Bandyopadhyay received the Ph.D degree in computer science and engineering from Indian Institute of Technology, Kharagpur in 2017. He had worked as a Junior Project Assistance in the VLSI Consortium project undertaken by the Advanced VLSI Design Laboratory, IIT Kharagpur from July 2008 to September 2012 and his current research interests include broadly formal methods in software engineering. He had received TCS Ph.D Fellowship during his Ph.D. He was working as a faculty member at BITS Goa campus from 2015 to July, 2017. From August 2017 to till date, he is working as a post doctoral fellow at System Analysis and Modeling group, Hasso Plattner Institute, Germany.

Dieser Gast wurde von Rolf Drechsler eingeladen.