Einladung zum Vortrag

19. April 2010, 16 Uhr c.t.
Universität Bremen | Cartesium | Rotunde

Tetsuya Iizuka
University of Tokyo

Buffer-Ring-Based All-Digital On-Chip Monitor for PMOS and NMOS Process Variability and Aging Effects

The improvement of VLSI process technologies over the last twenty years enables the integration of a large number of transistors on a single chip, and significantly improves the circuit performance. However, VLSI design and verification processes have become more and more complex. Moreover, a smaller feature sizes degrade the tolerance to the PVT (Process, Voltage, and Temperature) variabilities and the reliability concerns such as Negative Bias Instability (NBTI) and Channel Hot Carrier (CHC) have become of critical importance to nanoscale transistors.

In this talk, we present an all-digital process variability and aging monitor which utilizes a simple buffer ring with a pulse counter. Using the proposed circuit in combination with a simple ring oscillator which monitors its oscillation period, we can calculate the rise and fall delay values and we can monitor the variability of PMOS and NMOS devices independently. The experimental results of the circuit simulation on 65nm CMOS process indicate the feasibility of the proposed monitoring circuit. The proposed monitoring technique is suitable not only for the on-chip process variability monitoring but also for the infield monitoring of aging effects such as NBTI and CHC.

Biography | Iizuka
Tetsuya Iizuka received the B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 2002, 2004, and 2007, respectively. Then he worked as a high-speed serial interface circuit designer for two years. He joined University of Tokyo again in 2009, and is currently an Assistant Professor at the VLSI Design and Education Center, University of Tokyo. His research interests include digitally-assisted analog circuits and VLSI computer-aided-design. He is a member of the Institute of Electrical and Electronics Engineers (IEEE).

Kunihiro Asada
University of Tokyo

Self-timed Circuits as Resilient LSIs for Process-Voltage-Temperature Variation

The operation of synchronous circuits, as widely used today, is becoming increasingly unstable caused by PVT variation. The conventional margin-based design approach pays a large overhead to guarantee the safe operation, especially for delay. Recently, semi-self-timed approaches have been proposed to mitigate these problems, where the circuits have an error recovery mechanism along with delay-fault detection/prediction circuits such as a double sampling of signals. These approaches, however, still need a timing margin, in which the delay variation should be confined.

The self-timed circuits, with a completion-detection mechanism, are ideally delay-fault free. The dual-rail logic, used in our research, is a promising candidate to realize the mechanism, where the PVT variation causes not the delay-fault but the minimum performance degradation. The dual-rail logic has an additional feature to detect permanent and intermittent logic faults due to its redundancy. In this talk two examples will be given; an experimental self-timed CPU resilient for PVT variation and a self-timed FPGA, which is inheriting not only the delay-fault free feature but also a high throughput performance realized by the extremely fine-grain pipeline architecture.

Biography | Asada
Kunihiro Asada received the B. S., M. S., and Ph.D. in electronic engineering from University of Tokyo in 1975, 1977, and 1980, respectively. In 1980 he joined the Faculty of Engineering, University of Tokyo, and became a lecturer, an associate professor and a professor in 1981, 1985 and 1995, respectively. From 1985 to 1986 he stayed in Edinburgh University as a visiting scholar supported by the British Council. From 1990 to 1992 he served as the first Editor of English version of IEICE (Institute of Electronics, Information and Communication Engineers of Japan) Transactions on Electronics. In 1996 he established VDEC (VLSI Design and Education Center) with his colleagues in University of Tokyo, which is a center to promote education and research of VLSI design in all the universities and colleges in Japan. He also served as the Chair of IEEE/SSCS Japan Chapter in 2001-2002 and the Chair of IEEE Japan Chapter Operation Committee in 2007-2008. He is currently in charge of the director of VDEC. His research interest is design and evaluation of integrated systems and component devices. He has published more than 400 technical papers in journals and conference proceedings. He has received best paper awards from IEICE (Institute of Electrical Engineers of Japan), IEICE and ICMTS and so on. He is a member of IEEE, IEICE and IEEJ.

Die Vortragenden wurden von Dr. Görschwin Fey und Prof. Dr. Rolf Drechsler eingeladen.
Prof. Dr. Rolf Drechsler 218-63932    Dr. Görschwin Fey    218-63944