



ICCAD 2021 CONFERENCE PROGRAM



München und die Alpen bei Föhn, München Tourismus, Tommy Lösch

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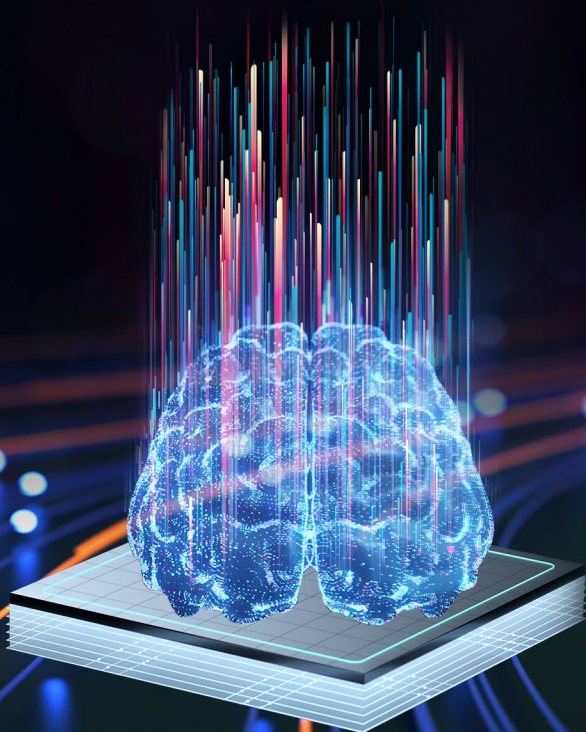
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WELCOME TO ICCAD 2021

It is our pleasure to welcome you to the 40th anniversary edition of the International Conference on Computer-Aided Design!

Since the global COVID-19 pandemic is still prevailing worldwide, the ICCAD 2021 Executive Committee decided to proceed with a virtualized solution for the conference in the second year from 1-4 November. A virtual conference leads to new challenges due to the missing personal interaction. However, the organizers are keen to provide an interesting program involving excellent technical contributions while also focusing on the networking aspects. In the end, we aim at creating a unique conference experience. For facilitating this plan, and thanks to the rapidly deployed vaccines and strict hygienic measures, ICCAD will be extended to offer a unique opportunity for an In-Person Networking Event in Munich, Germany, on 5 November. This one-day event will focus on networking to mitigate the effects of the missing personal exchange.

Jointly sponsored by ACM and IEEE, ICCAD is the premier forum to explore emerging technology challenges in electronic design automation, present leading-edge R&D solutions, and identify emerging technologies for design automation research areas. The members of the executive committee, the technical program committee, and numerous volunteers have spent an enormous effort to prepare an outstanding technical program.

We are glad to announce that we again had a significant increase in the number of regular paper submissions with 514 papers going through the complete review peer-review process. This strong submission record amidst a global pandemic emphasizes the high relevance and the recognition of the conference within, but not limited to, the CAD community. For handling such an enormous submission number, we have carefully created 15 tracks and invited outstanding technical program committee members from both industry and academia worldwide for each track.

The TPC meeting was conducted again as an online event without compromising the quality of the double-blind review process. Finally, the program committee has selected 121 papers yielding 32 regular sessions on diverse topics. Altogether, we have nine special sessions and three embedded tutorials on topics that complement the regular sessions.

We are delighted to present four distinguished keynote speakers: the Monday morning keynote on Efficient Computing for AI and Robotics will be given by Professor Vivienne Sze from the Massachusetts Institute of Technology. On Tuesday, Professor Elison Matioli from the Ecole Polytechnique Fédérale de Lausanne will present the IEEE CEDA Luncheon Distinguished Lecture on challenges and opportunities in GaN power electronics. Furthermore, Professor David Patterson from the University of California, Berkeley will present the Wednesday keynote on the RISC-V architecture. Finally, during the ICCAD's Networking In-Person event on Friday, Dr. Dirk Ziegenbein from Robert Bosch GmbH will give an in-person keynote on the design of reliable distributed systems. We hope you will find these keynotes exciting and informative.

On Thursday, we have six interesting workshops on various new and established topics. Some of these workshops are long-time staples of ICCAD, while others test the waters for the first time. Additionally, a further workshop addressing System-level interconnect problems is co-located with ICCAD. We hope that you will join the workshops offering an exciting program.

Please let me emphasize again that ICCAD aims relentlessly at being the ultimate destination for cutting-edge EDA research and emerging CAD technologies. We appreciate your attendance and your support in shaping this virtual event into a memorable one. Finally, we are grateful to our ICCAD 2021 sponsors and numerous supporters for making this year's conference another successful event.



General Chair

Rolf Drechsler

University of Bremen/DFKI

A handwritten signature in blue ink, appearing to read 'Rolf Drechsler'.

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GENERAL INFORMATION

PROCEEDINGS

Please download the ICCAD 2021 Proceedings zip folder. Once you have it on your computer, you will need to extract the files from the zip folder. Then you will be able to see the content

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CONFERENCE MANAGEMENT



Conference Catalysts' mission is to provide world-class conference management, operations management, and web & graphics solutions with a superior level of service and an individualized approach based on our clients' specific needs.



Marienplatz Panorama, München Tourismus, Jörg Lutz

BEST PAPER CANDIDATES

IEEE/ACM William J. McCalla ICCAD Best Paper Award Candidates

Session 10C: Bounded Model Checking of Speculative Non-Interference

Emmanuel Pescosta, Georg Weissenbacher, Florian Zuleger

Session 5B: DeepFreeze: Cold Boot Attack and Model Recovery on Commercial EdgeML Device

Yoo-Seung Won, Soham Chatterjee, Dirmanto Jap, Shivam Bhasin, Arindam Basu

Session 2D: BOOM-Explorer: RISC-V BOOM Microarchitecture Design Space Exploration Framework

Chen BAI, Qi SUN, Jianwang Zhai, Yuzhe Ma, Bei Yu, Martin Wong

Session 11C: Analytical Modeling of Transient Electromigration Stress based on Boundary Reflections

Mohammad Abdullah Al Shohel, Vidya Chhabria, Nestor Evmorfopoulos, Sachin S. Sapatnekar

Session 1B: Engineering an Efficient Boolean Functional Synthesis Engine

Priyanka Golia, Friedrich Slivovsky, Subhajit Roy, Kuldeep S Meel

Session 11B: pGRASS-Solver: A Parallel Iterative Solver for Scalable Power Grid Analysis Based on Graph Spectral Sparsification

Zhiqiang Liu, Wenjian Yu

BEST PAPER AWARD COMMITTEES

IEEE/ACM William J. McCalla ICCAD Best Paper Award Selection Committee

Laleh Behjat (Chair) - University of Calgary

Ulf Schlichtmann - Technical University of Munich

C.K. Cheng - University of California, San Diego

Jie-Hong Roland Jiang - National Taiwan University

Ramesh Karri - New York University

Tei-Wei Kuo - City University of Hong Kong

ICCAD TEN-YEAR RETROSPECTIVE MOST INFLUENTIAL PAPER COMMITTEE:

Ting-Chi Wang (Chair) - National Tsing Hua University

Yiran Chen - Duke University

Jiang Hu - Texas A&M University

Takashi Sato - Kyoto University

Ulf Schlichtmann - Technical University of Munich

EMBEDDED TUTORIAL/SPECIAL SESSION COMMITTEE

Jinjun Xiong (Chair) - University at Buffalo

Sachin Sapatnekar - University of Minnesota

Tony Givargis - University of California, Irvine

Laleh Behjat - University of Calgary

Wenjian Yu - Tsinghua University

Yiyu Shi - University of Notre Dame

Iris Hui-Ru Jiang - National Taiwan University

KEYNOTE SPEAKERS

MONDAY, NOVEMBER 1



Keynote: Efficient Computing for AI and Robotics: From Hardware Accelerators to Algorithm Design

Time: 8:00 AM – 9:00 AM UTC-7

Speaker: Vivienne Sze, Massachusetts Institute of Technology (MIT)

Abstract: The compute demands of AI and robotics continue to rise due to the rapidly growing volume of data to be processed; the increasingly complex algorithms for higher quality of results; and the demands for energy efficiency and real-time performance. In this talk, we will discuss the design of efficient hardware accelerators and the co-design of algorithms and hardware that reduce the energy consumption while delivering real-time and robust performance for applications including deep neural networks and autonomous navigation. We will also highlight important design principles, methodologies, and tools that can facilitate an effective design process.

Biography: Vivienne Sze (<http://sze.mit.edu/>) is an associate professor in MIT's Department of Electrical Engineering and Computer Science and leads the Research Lab of Electronics' Energy-Efficient Multimedia Systems research group. Her group works on computing systems that enable energy-efficient machine learning, computer vision, and video compression/processing for a wide range of applications, including autonomous navigation, digital health, and the internet of things. She is widely recognized for her leading work in these areas and has received many awards, including faculty awards from Google, Facebook, and Qualcomm, the Symposium on VLSI Circuits Best Student Paper Award, the IEEE Custom Integrated Circuits Conference Outstanding Invited Paper Award, and the IEEE Micro Top Picks Award. As a member of the Joint Collaborative Team on Video Coding, she received the Primetime Engineering Emmy Award for the development of the High-Efficiency Video Coding video compression standard. She is a co-author of the book entitled "[Efficient Processing of Deep Neural Networks](#)".

KEYNOTE SPEAKERS

TUESDAY, NOVEMBER 2 (CEDA KEYNOTE)



Keynote: Challenges and opportunities in GaN power electronics

Time: 8:00 AM – 9:00 AM UTC-7

Speaker: Elisa Matioli, Ecole Polytechnique Fédérale de Lausanne (EPFL)

Abstract: Electricity is the fastest growing form of end-use energy, however a considerable portion of the electricity consumed worldwide is wasted in power conversion, especially in power semiconductor devices. The outstanding properties of Gallium Nitride and other widebandgap semiconductors for power electronic devices can enable significantly more efficient and compact future power converters. These devices are currently becoming ubiquitous in power electronic circuits, however due to their different physical process compared to common power electronic devices, there is a lack of proper compact modeling tools that correctly represent their behavior under different conditions as well as computer-aided design and optimization approaches to automatically optimize the device design. This talk will present the principles, state-of-the-art and challenges of GaN power devices for efficient power conversion, aiming to open opportunities for device modeling and automation in the field of power electronics.

Biography: Elisa Matioli is a professor in the institute of electrical engineering at Ecole Polytechnique Fédérale de Lausanne (EPFL), since 2015. He received a B.Sc. degree in applied physics and applied mathematics from Ecole Polytechnique (Palaiseau, France), followed by a Ph.D. degree from the Materials Department at the University of California, Santa Barbara (UCSB) in 2010. He was a post-doctoral fellow in the EECS department at the Massachusetts Institute of Technology (MIT) until 2014. He has received the UCSB Outstanding Graduate Student – Scientific Achievement Award for his Ph.D. work, the 2013 IEEE George Smith Award, the 2015 ERC Starting Grant Award, the 2016 SNSF Assistant Professor Energy Grant Award and the 2020 University Latsis Prize.

KEYNOTE SPEAKERS

WEDNESDAY, NOVEMBER 3



Keynote: RISC-V Is Inevitable

Time: 8:00 AM – 9:00 AM UTC-7

Speaker: David Patterson, University of California, Berkeley

Abstract: This talk reviews the history, current state, and future directions of RISC-V (“RISC Five”), an open instruction set architecture that is growing in commercial significance. It covers:

1. Novel features of the recent instruction set extensions, such as vector and bit manipulation;
2. Compares their efficiency to conventional proprietary instruction sets; and
3. Gives examples of advances in computer security due to the open instruction set by allowing anyone to test their ideas end-to-end via red team attacks over the Internet on full scale hardware/software systems based on novel architecture features implemented via FPGAs that can be iterated weekly.

Biography: David Patterson is a UC Berkeley professor, Google distinguished engineer, RISC-V International Vice-Chair, and RISC-V International Open Source Laboratory Director. His best-known projects are RISC and RAID. He co-authored seven books, including *Computer Architecture: A Quantitative Approach*, and shared the 2017 ACM A.M Turing Award shared with his co-author John Hennessy.

KEYNOTE SPEAKERS

FRIDAY, NOVEMBER 5 (IN PERSON)



Keynote: Designing Reliable Distributed Systems

Time: 11:00 AM - 12:00 AM CET

Speaker: Dirk Ziegenbein, Robert Bosch GmbH

Abstract: Software is disrupting one industry after the other. Currently, the automotive industry is feeling the pinch to innovate in the software business. New, innovative approaches to vehicles and their HW/SW architectures are needed and are currently subsumed under the term SW-defined Vehicle. This trend however does not stop at vehicle boundaries but includes off-board communication with edge and cloud services. Thinking it further, this results in a disruptive technology we call Reliable Distributed Systems (RDS), enabling the operation of vehicles, where parts, such as sensing and compute are no longer bound to the vehicle, but can be performed in an edge-cloud continuum. Reliable Distributed Systems are not limited to automotive use cases. By making compute and sensing ubiquitously available, as well as offering transparent communications, applications in several domains are possible: from industrial automation, over building automation to consumer robotics. However, designing Reliable Distributed Systems raises several questions and poses new challenges for electronic design automation.

Biography: Dirk Ziegenbein is chief expert for open context systems engineering and leads a research group developing methods and technologies for software systems engineering at Bosch Corporate Research in Stuttgart, Germany. He held several positions in R&D (software component technology, scheduling analysis and software architectures for multi-cores) and product management (embedded software engineering tools). Dirk is an initiator of the DATE Special Initiative on Autonomous Systems Design.

MONDAY SCHEDULE

Join the ICCAD Gather Space to network and continue asking questions (for 30 minutes after each session concludes)

7:20 – 8:00AM 4:20 - 5PM CET (GERMANY), 10:20 - 11PM CST (CHINA)

Opening Session & Awards

8:00 – 9:00AM 5 - 6PM CET (GERMANY), 11PM - 12AM CST (CHINA)

Keynote: Efficient Computing for AI and Robotics: From Hardware Accelerators to Algorithm Design

Vivienne Sze, Massachusetts Institute of Technology

9:00 – 9:30AM 6 - 6:30PM CET (GERMANY), 12AM - 12:30AM CST (CHINA)

1A: Efficient DNN Training and Secure/Robust DNN Inference

1B: Advances in Boolean Methods for Synthesis

1C: Power Model Calibration and Computing with Approximation and Uncertainty

Session 1D | Special Session: Cross Layer Design Solutions for Energy-Efficient and Secure Edge AI

9:45 – 10:15AM 6:45 - 7:15PM CET (GERMANY), 12:45 - 1:15AM CST (CHINA)

2A: Efficient DNN Inference and Tools

2B: LOLOL: Lots of Logic Locking and Unlocking

2C: Quantum CAD Matters

2D: Multi-Core System Design and Optimization for the Big Data Era

10:30 – 11:00AM 7:30 - 8PM CET (GERMANY), 1:30 - 2AM CST (CHINA)

3A: Algorithm-Hardware Co-Design for Machine Learning Hardware Accelerators

3B: Routing with Wires and Light

3C: CAD for Novel Electronic Applications

Session 3D | Special Session: Quantum Machine Learning: From Algorithm to Applications

11:00 – 1:00PM 8 - 10:00PM CET (GERMANY), 2 - 4:00AM CST (CHINA)

ACM Student Research Contest

OPENING SESSION & AWARDS

7:20 – 8:00am

ICCAD 2021 Ten Year Retrospective Most Influential Paper Award:

“MACACO: Modeling and Analysis of Circuits for Approximate Computing” (appeared in ICCAD 2011) by **Rangharajan Venkatesan, Amit Agarwal, Kaushik Roy, and Anand Raghunathan**

ICCAD 2021 William J. McCalla ICCAD Best Paper Award (Front End):

BOOM-Explorer: RISC-V BOOM Microarchitecture Design Space Exploration Framework by **Chen BAI, Qi Sun, Jianwang Zhai, Yuzhe Ma, Bei Yu, Martin Wong**

Session: 2D – November 01, 9:45am UTC-7

ICCAD 2021 William J. McCalla ICCAD Best Paper Award (Back End):

Analytical Modeling of Transient Electromigration Stress based on Boundary Reflections by **Mohammad Abdullah Al Shohel, Vidya A. Chhabria, Nestor Evmorfopoulos, Sachin S. Sapatnekar**

Session: 2D – November 03, 10:30am UTC-7



Olympiapark, München, Germany, Unsplash, Kostya Golinchenko

1A – EFFICIENT DNN TRAINING AND SECURE/ROBUST DNN INFERENCE

Time: 9:00 AM – 9:45 AM

Moderator: Yingyan Lin, Rice University

Deep neural networks (DNNs) have achieved tremendous performance breakthroughs. However, the development and application of DNNs still face various challenges. For example, DNNs' powerful performance comes at a prohibitive training cost, and DNN inference can suffer from security/robustness issues. This session introduces techniques towards efficient DNN training and secure/robust DNN inference.

Lower Voltage for Higher Security: Using Voltage Overscaling to Secure Deep Neural Networks

Md Shohidul Islam, George Mason University

Ihsen Alouani, IEMN lab, INSA Hauts-de-France, Université Polytechnique Hauts-De-France

Khaled N. Khasawneh, George Mason University

Deferred Dropout: An Algorithm-Hardware Co-Design DNN Training Method Provisioning Consistent High Activation Sparsity

Kangkyu Park, Korea Advanced Institute of Science and Technology

Yunki Han, Korea Advanced Institute of Science and Technology

Lee-Sup Kim, Korea Advanced Institute of Science and Technology

LayerPipe: Accelerating Deep Neural Network Training by Intra-Layer and Inter-Layer Gradient Pipelining and Multiprocessor Scheduling

Nanda Unnikrishnan, University of Minnesota

Keshab Parhi, University of Minnesota

Multi-Objective Optimization of ReRAM Crossbars for Robust DNN Inferencing under Stochastic Noise

Xiaoxuan Yang, Duke University

Syrine Belakaria, Washington State University

Biresh Kumar Joardar, Duke University

Huanrui Yang, Duke University

Jana Doppa, Washington State University

Partha Pratim Pande, Washington State University

Krishnendu Chakrabarty, Duke University

Hai (Helen) Li, Duke University

1B – ADVANCES IN BOOLEAN METHODS FOR SYNTHESIS

Time: 9:00 AM – 9:45 AM

Moderator: Cheng Tan, Pacific Northwest National Laboratory

This session introduces the latest progress in Boolean methods for synthesis. The first paper describes algorithmic improvements for a data-driven framework for functional synthesis. The second paper exploits Boolean sensitivity to enhance Boolean matching. The third paper presents a two-phase approach for prime compilation of non-clausal formulae. The last paper shows an approximate two-level logic minimization technique scalable up to millions of minterms.

Engineering an Efficient Boolean Functional Synthesis Engine

Priyanka Golia, Indian Institute of Technology Kanpur, National University of Singapore

Friedrich Slivovsky, TU Wien

Subhajit Roy, Indian Institute of Technology Kanpur

Kuldeep S Meel, National University of Singapore

Enhanced Fast Boolean Matching based on Sensitivity Signatures Pruning

Jiaxi Zhang, Peking University

Liwei Ni, Pengcheng Laboratory

Shenggen Zheng, Pengcheng Laboratory

Hao Liu, Peking University

Xiangfu Zou, Pengcheng Laboratory

Feng Wang, Peking University

Guojie Luo, Peking University

An Efficient Two-Phase Method for Prime Compilation of Non-Clausal Boolean Formulae

Weilin Luo, Sun Yat-sen University

Hai Wan, Sun Yat-sen University

Hongzhen Zhong, Sun Yat-sen University

Ou Wei, University of Toronto

Biqing Fang, Sun Yat-sen University

Xiaotong Song, Sun Yat-sen University

Heuristics for Million-scale Two-level Logic Minimization

Mahdi Nazemi, University of Southern California

Hitarth Kanakia, University of Southern California

Massoud Pedram, University of Southern California

1C – POWER MODEL CALIBRATION AND COMPUTING WITH APPROXIMATION AND UNCERTAINTY

Time: 9:00 AM – 9:45 AM

Moderator: Seda Ogrenci-Memik, Northwestern University

This session presents papers on adapting power modeling and circuit design in the presence of variability, approximation, and uncertainty. The first paper describes a method for calibrating architecture dependent power models in consideration of workload characteristics. The following paper addresses design of arithmetic units optimized for approximate computing. The session is concluded with two works that address stochastic computing paradigms. These papers address automated design of replacing complex designs with simplified stochastic surrogates and manipulating correlation characteristics of inputs to stochastic circuits, respectively.

McPAT-Calib: A Microarchitecture Power Modeling Framework for Modern CPUs

Jianwang Zhai, Tsinghua University
Chen Bai, The Chinese University of Hong Kong
Binwu Zhu, The Chinese University of Hong Kong
Yici Cai, Tsinghua University
Qiang Zhou, Tsinghua University
Bei Yu, The Chinese University of Hong Kong

Positive/Negative Approximate Multipliers for DNN Accelerators

Ourania Spantidi, Southern Illinois University Carbondale
Georgios Zervakis, Karlsruhe Institute of Technology
Iraklis Anagnostopoulos, Southern Illinois University Carbondale
Hussam Amrouch, University of Stuttgart
Joerg Henkel, Institut für Technologie (KIT)

MinSC: An Exact Synthesis-Based Method for Minimal Area Stochastic Circuits under Relaxed Error Bound

Xuan Wang, Shanghai Jiao Tong University
Zhufei Chu, Ningbo University
Zhufei Chu, Ningbo University
Weikang Qian, Shanghai Jiao Tong University

CORLD: In-Stream Correlation Manipulation for Low-Discrepancy Stochastic Computing

Sina Asadi, University of Louisiana at Lafayette
M. Hassan Najafi, University of Louisiana at Lafayette
Mohsen Imani, UC Irvine

SPECIAL SESSION 1D – CROSS LAYER DESIGN SOLUTIONS FOR ENERGY-EFFICIENT AND SECURE EDGE AI

Time: 9:00 AM – 9:45 AM

Moderator: Muhammad Shafique, New York University Abu Dhabi

This special session will articulate the challenges associated with creating energy-efficient and secure Edge AI as well as highlight opportunities for deriving the maximum possible benefit from cross-layer design of both hardware and software. The presenters will describe the most-compelling research advances in cross-layer design solutions that will allow us to push the Pareto front of energy, performance, accuracy, and privacy with current approaches. This special session will consist of four talks, which will cover different important topics on EdgeAI, like tinyML, energy efficiency, security and reliability, and Hardware-Software Co-design.

TinyML: Massive Opportunity for Edge AI when Machine Intelligence meets the Real World of Billions of Sensors *(Invited Paper)*

Evgeni Gousev, Qualcomm Technologies, Inc.

Challenges and Opportunities in Security and Reliability of Edge AI *(Invited Paper)*

Aviv Barkai, Intel

A General Hardware and Software Co-Design Framework for Energy-Efficient Edge AI *(Invited Paper)*

Nitthilan Kannappan Jayakodi, Washington State University
Janardhan Rao Doppa, Washington State University
Partha Pratim Pande, Washington State University

Towards Energy-Efficient and Secure Edge AI: A Cross-Layer Framework *(Invited Paper)*

Muhammad Shafique, New York University Abu Dhabi
Alberto Marchisio, TU Wien
Rachmad Vidya Wicaksana Putra, TU Wien
Muhammad Abdullah Hanif, TU Wien

2A – EFFICIENT DNN INFERENCE AND TOOLS

Time: 9:45 AM – 10:30 AM

Moderator: Ziyun Li, Facebook

Recent successes of Deep neural networks (DNNs) have motivated a growing interest in DNN powered inference and tools. This session introduces efficient DNN inference techniques and DNN-based congestion prediction. The former is to close the gap between DNNs' prohibitive complexity and resource constrained devices, while the latter aims to leverage DNNs for predicting cell congestion during logic synthesis.

Bit-Transformer: Transforming Bit-level Sparsity into Higher Performance in ReRAM-based Accelerator

Fangxin Liu, Shanghai Jiao Tong University
Wenbo Zhao, Shanghai Jiao Tong University
Zhezhi He, Shanghai Jiao Tong University
Zongwu Wang, Shanghai Jiao Tong University
Yilong Zhao, Shanghai Jiao Tong University
Yongbiao Chen, Shanghai Jiao Tong University
Li Jiang, Shanghai Jiao Tong University

Crossbar based Processing in Memory Accelerator Architecture for Graph Convolutional Networks

Nagadastagiri Challapalle, The Pennsylvania State University
Karthik Swaminathan, IBM T.J Watson Research Center
Nandhini Chandramoorthy, IBM Research
Vijaykrishnan Narayanan, Penn State University

Evolving Complementary Sparsity Patterns for Hardware-Friendly Inference of Sparse DNNs

Elbruz Ozen, University of California, San Diego
Alex Orailoglu, University of California, San Diego

Generalizable Cross-Graph Embedding for GNN-based Congestion Prediction

Amur Ghose, Huawei
Vincent Zhang, Huawei
Yingxue Zhang, Huawei Noah's Ark Lab, Huawei Technologies Canada
Dong Li, Huawei
Wulong Liu, Huawei Noah's Ark Lab
Mark Coates, McGill University

2B – LOLOL: LOTS OF LOGIC LOCKING AND UNLOCKING

Time: 9:45 AM – 10:30 AM

Moderator: Sri Parameswaran, The University of New South Wales

Logic Locking is being promoted as a defense against the threat of intellectual property piracy. This session explores the benefits of power side channels in unlocking a locked circuit, application of machine learning in unlocking, the locking benefits of embedded FPGAs. The last paper of this session examines security of Multi-Tenant FPGAs.

UNTANGLE: Unlocking Routing and Logic Obfuscation Using Graph Neural Networks-based Link Prediction

Lilas Alrahis, New York University Abu Dhabi

Satwik Patnaik, Texas A&M University

Muhammad Hanif, Vienna University of Technology

Muhammad Shafique, New York University Abu Dhabi

Ozgur Sinanoglu, New York University Abu Dhabi

Circuit Deobfuscation from Power Side-Channels using Pseudo-Boolean SAT

Kaveh Shamsi, University of Texas at Dallas

Yier Jin, University of Florida

Exploring eFPGA-based Redaction for IP Protection

Jitendra Bhandari, New York University

Abdul Khader Thalakkattu Moosa, New York University

Benjamin Tan, New York University

Christian Pilato, Politecnico di Milano

Ganesh Gore, University of Utah

Xifan Tang, University of Utah

Scott Temple, University of Utah

Pierre-Emmanuel Gaillardon, University of Utah

Ramesh Karri, New York University

LoopBreaker: Disabling Interconnects to Mitigate Voltage-Based Attacks in Multi-Tenant FPGAs

Hassan Nassar, Karlsruher Institut für Technologie

Hanna AlZughbi, Independent

Dennis Gnad, Karlsruher Institut für Technologie

Lars Bauer, Karlsruher Institut für Technologie

Mehdi Tahoori, Karlsruher Institut für Technologie

Jörg Henkel, Karlsruher Institut für Technologie

2C – QUANTUM CAD MATTERS

Time: 9:45 AM – 10:30 AM

Moderator: Anupam Chattopadhyay, Nanyang Technological University

This session brings four exciting contributions from the domain of Quantum technologies, which promises to advance the field of computing with breakthrough algorithms. The first paper presents an optimal mapping for Quantum architectures, while the second one proposes an optimal algorithm for inserting splitters and buffers for AQFP circuits. The third paper tackles the clock tree synthesis problem for SFQ circuits. The last paper sheds light on the security challenges of Quantum circuits.

Optimal Mapping for Near-Term Quantum Architectures based on Rydberg Atoms

Sebastian Brandhofer, University of Stuttgart

Hans Peter Büchler, University of Stuttgart

Ilia Polian, University of Stuttgart

An Optimal Algorithm for Splitter and Buffer Insertion in Adiabatic Quantum-Flux-Parametron Circuits

Chao-Yuan Huang, National Tsing Hua University

Yi-Chen Chang, Department of Computer Science, National Tsing Hua University

Ming-Jer Tsai, Department of Computer Science, National Tsing Hua University

Tsung-Yi Ho, Department of Computer Science, National Tsing Hua University

A Novel Clock Tree Aware Placement Methodology for Single Flux Quantum (SFQ) Logic Circuits

Ching-Cheng Wang, National Tsing Hua University

Wai-Kei Mak, National Tsing Hua University

Split Compilation for Security of Quantum Circuits

Abdullah Ash-Saki, Pennsylvania State University

Aakarshitha Suresh, Pennsylvania State University

Rasit Onur Topaloglu, IBM

Swaroop Ghosh, Pennsylvania State University

2D – MULTI-CORE SYSTEM DESIGN AND OPTIMIZATION FOR THE BIG DATA ERA

Time: 9:45 AM – 10:30 AM

Moderator: Katzalin Olcoz Herrero, Complutense University of Madrid

In this session, we cover the latest trends on system-level microarchitecture and memory subsystem design and optimization targeting the new types of machine learning and deep learning (ML/DL) applications. The first two papers cover new design and optimization frameworks for many-core systems to be adapted to different types of ML/DL applications. The last two deal with new methods to model and optimize the behavior of processing and communication subsystems in multi-core platforms according to the characteristics of the latest applications in the Big Data Era. In this session, we cover the latest trends on system-level microarchitecture and memory subsystem design and optimization targeting the new types of machine learning and deep learning (ML/DL) applications. The first two papers cover new design and optimization frameworks for many-core systems to be adapted to different types of ML/DL applications. The last two deal with new methods to model and optimize the behavior of processing and communication subsystems in multi-core platforms according to the characteristics of the latest applications in the Big Data Era.

BOOM-Explorer: RISC-V BOOM Microarchitecture Design Space Exploration Framework *(BPA award winner)*

Chen Bai, The Chinese University of Hong Kong

Qi Sun, The Chinese University of Hong Kong

Jianwang Zhai, Tsinghua University

Yuzhe Ma, The Chinese University of Hong Kong

Bei Yu, The Chinese University of Hong Kong

Martin Wong, The Chinese University of Hong Kong

DARe: DropLayer-Aware Manycore ReRAM architecture for Training Graph Neural Networks

Aqeeb Iqbal Arka, Washington State University

Bires Kumar Joardar, Duke University

Jana Doppa, Washington State University

Partha Pratim Pande, Washington State University

Krishnendu Chakrabarty, Duke University

IPA: Floorplan-Aware SystemC Interconnect Performance Modeling and Generation for HLS-based SoCs

Nathaniel Pinckney, NVIDIA Corporation

Rangharajan Venkatesan, NVIDIA Corporation

Ben Keller, NVIDIA Corporation

Brucek Khailany, NVIDIA Corporation

Theoretical Analysis and Evaluation of NoCs with Weighted Round Robin Arbitration

Sumit Mandal, University of Wisconsin-Madison

Jie Tong, University of Wisconsin-Madison

Raid Ayoub, Intel Corporation

Michael Kishinevsky, Intel Corporation

Ahmed Abousamra, Intel Corporation

Umit Ogras, University of Wisconsin – Madison

3A – ALGORITHM-HARDWARE CO-DESIGN FOR MACHINE LEARNING HARDWARE ACCELERATORS

Time: 10:30 AM – 11:00 AM

Moderator: Nagarajan Kandasamy, Drexel University

The session explores novel hardware-software co-design techniques for next-generation computing system design enabled by emerging device technologies. The technical papers are driven by algorithmic insights ranging from Bayesian neural networks, residue number systems to novel applications like personalized recommendation systems.

Reliable Memristor-based Neuromorphic Design Using Variation- and Defect-Aware Training

Di Gao, Zhejiang University

Grace Li Zhang, Technical University of Munich

Xunzhao Yin, Zhejiang University

Bing Li, Technical University of Munich

Ulf Schlichtmann, Technical University of Munich

Cheng Zhuo, Zhejiang University

REREC: In-ReRAM Acceleration with Access-Aware Mapping for Personalized Recommendation

Yitu Wang, Duke University

Zhenhua Zhu, Tsinghua University

Fan Chen, Indiana University

Mingyuan Ma, Duke University

Guohao Dai, Tsinghua University

Yu Wang, Tsinghua University

Hai (Helen) Li, Duke University

Yiran Chen, Duke University

RNSim: Efficient Deep Neural Network Accelerator Using Residue Number Systems

Arman Roohi, University of Nebraska – Lincoln

MohammadReza Taheri, Independent Researcher

Shaahin Angizi, New Jersey Institute of Technology

Deliang Fan, Arizona State University

3B – ROUTING WITH WIRES AND LIGHT

Time: 10:30 AM – 11:00 AM

Moderator: Mehmet Yildiz, Cadence Design Systems

This session covers several different routing related papers. The first paper assigns signals between FPGAs in a multi-FPGA emulation system with Time -division multiplexing utilizing limited I/O bandwidth, to achieve the maximum clock frequency for the emulation system. The second paper proposes using an integer linear program to assign optical wave guides routes across a hexagonal grid to minimize transmission loss, while supporting waveguide matching constraints. The last paper proposes a sweep-style algorithm for GPU-accelerated parallel maze routing for global routing.

Time-Division Multiplexing Based System-Level FPGA Routing

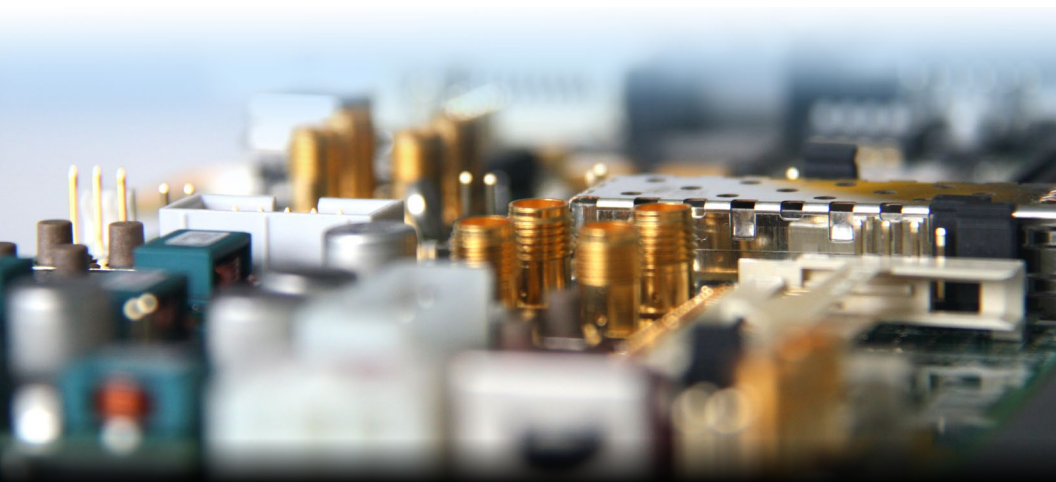
Wei-Kai Liu, National Taiwan University
Ming-Hung Chen, National Taiwan University
Chia-Ming Chang, National Taiwan University
Chen-Chia Chang, National Taiwan University
Yao-Wen Chang, National Taiwan University

Optical Routing Considering Waveguide Matching Constraints

Fu-Yu Chuang, National Taiwan University
Yao-Wen Chang, National Taiwan University

GAMER: GPU Accelerated Maze Routing

Shiju Lin, The Chinese University of Hong Kong
Jinwei Liu, The Chinese University of Hong Kong
Martin Wong, The Chinese University of Hong Kong



3C – CAD FOR NOVEL ELECTRONIC APPLICATIONS

Time: 10:30 AM – 11:00 AM

Moderator: Shaloo Rakheja, University of Illinois at Urbana-Champaign

CAD has been a key enabler of CMOS integration. It is now being applied to new electronic applications and has a strong potential to address specific challenges of these technologies. The first paper of this session applies CAD techniques to avoid printing issues and improve the manufacturing efficiency of ink jet printed electronics. In the second paper, the problem of parasitic carbon nanotubes connecting different cells together is resolved by rotating selected ones. The session will close with a presentation of an efficient layout synthesis algorithm for 2D and 3D power modules, thus addressing an important and open research need in the power electronics society.

Manufacturing Cycle-Time Optimization Using Gaussian Drying Model for Inkjet-Printed Electronics

Tsun-Ming Tseng, Technical University of Munich

Meng Lian, Technical University of Munich

Mengchu Li, Technical University of Munich

Philipp Rinklin, Technical University of Munich

Leroy Grob, Technical University of Munich

Bernhard Wolfrum, Technical University of Munich

Ulf Schlichtmann, Technical University of Munich

ParaMiE: Mitigating Parasitic CNFETs in the Presence of Unetched CNTs

Sanmitra Banerjee, Duke University

Arjun Chaudhuri, Duke University

Jinwoo Kim, Georgia Institute of Technology

Gauthaman Murali, Georgia Institute of Technology

Mark Nelson, SkyWater Technology

Sung Kyu Lim, Georgia Tech

Krishnendu Chakrabarty, Duke University

Hierarchical Layout Synthesis and Optimization Framework for High-Density Power Module Design Automation

Imam Al Razi, University of Arkansas

Quang Le, University of Arkansas

H. Alan Mantooth, University of Arkansas

Yarui Peng, University of Arkansas

SPECIAL SESSION 3D – QUANTUM MACHINE LEARNING: FROM ALGORITHM TO APPLICATIONS

Time: 10:30 AM – 11:00 AM

Moderator: Rasit Onur Topaloglu, IBM

This special session will provide insights on building scalable QML circuits, training them and finally exploiting them to solve socially relevant combinatorial optimization applications including finance and image classification using noisy quantum computers.

Quantum Variational Methods for Quantum Applications *(Invited Paper)*

Xiaodi Wu, University of Maryland

Mode connectivity in the QCBM loss landscape: ICCAD Special Session Paper *(Invited Paper)*

Kathleen Hamilton, Oak Ridge National Lab

Emily Lynn

Vicente Leyton-Ortega

Swarnadeep Majumder

Raphael Pooser

Quantum Machine Learning for Finance *(Invited Paper)*

Marco Pistoia, JPMorgan Chase

Quantum-Classical Hybrid Machine Learning for Image Classification *(Invited Paper)*

Mahabubul Alam, Pennsylvania State University

Satwik Kundu, Pennsylvania State University

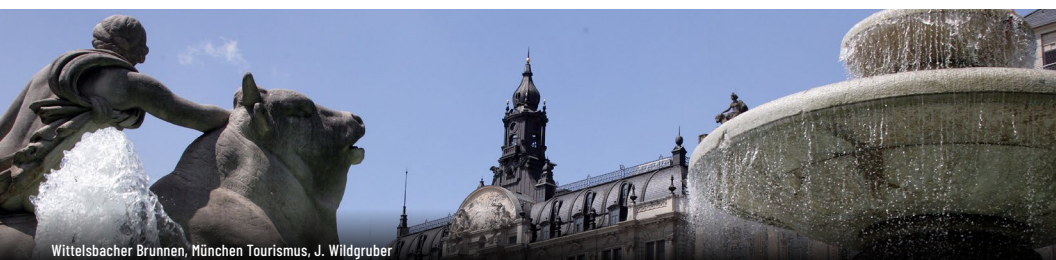
Rasit Topaloglu, IBM

Swaroop Ghosh, Pennsylvania State University

ACM STUDENT RESEARCH CONTEST

Time: 11:00 AM – 1:00 PM

Organizers: Meng Li, Facebook; **Cong Hao**, Georgia Institute of Technology



Wittelsbacher Brunnen, München Tourismus, J. Wildgruber

TUESDAY SCHEDULE

Join the ICCAD Gather Space to network and continue asking questions (for 30 minutes after each session concludes)

7:20 – 8:00AM 4:20 - 5PM CET (GERMANY), 10:20 - 11PM CST (CHINA)

4A: Acceleration of Emerging Deep Learning Techniques

4B: Resilient and Efficient Embedded Applications

4C: Simulation and Test Generation Tools

Special Session 4D: VLSI for 5G and Beyond Wireless in the AI Era: Algorithm, Hardware and System

8:00 – 9:00AM 5 - 6PM CET (GERMANY), 11PM - 12AM CST (CHINA)

IEEE CEDA Keynote: Challenges and opportunities in GaN power electronics

Elison Matioli, Ecole Polytechnique Fédérale de Lausanne

9:00 – 9:45AM 6 - 6:45PM CET (GERMANY), 12 - 12:45AM CST (CHINA)

5A: Hardware Software Co-Design for Advanced Deep Neural Networks

5B: Security of ML systems

5C: Managing Complexity with Cell Design and Partitioning

Session 5D | Tutorial: Hardware Aware Learning for Medicine

9:45 – 10:30AM 6:45 - 7:30PM CET (GERMANY), 12:45 - 1:30AM CST (CHINA)

6A: Brain-Inspired Computing and Microfluidic Bio-chips

6B: New Techniques in Timing and Power Analysis

6C: Machine Learning Methods for DFM

Session 6D | Tutorial: Ferroelectric FET Technologies and Its Applications: from Device to System

10:30 – 11:00AM 7:30 - 8PM CET (GERMANY), 1:30 - 2AM CST (CHINA)

7A: In-Memory Computing Circuits and Architectures

7B: Techniques Towards Fully Automated Analog IC Designs

Special Session 7C: Big Data, Big Deal: Data Analysis and Smart Tuning of EDA Flows

Session 7D | Tutorial: Optimizing and Mapping Quantum Algorithms to Quantum Computers in NISQ Era

11:00 – 12:00PM 8 - 9PM CET (GERMANY), 2 - 3AM CST (CHINA)

Cadence Sponsor Session: "Charting the Path to 3nm & More than Moore"

Rod Metcalfe, Cadence Design Systems

4A – ACCELERATION OF EMERGING DEEP LEARNING TECHNIQUES

Time: 7:20 AM – 8:00 AM

Moderator: Janardhan Rao Doppa, Washington State University

This session presents different techniques for accelerating emerging deep learning techniques, ranging from optical neural networks to BERT execution on ReRAM architectures. The first paper presents an automated optical hardware accelerator architecture for boosting the acceleration efficiency and development speed of optical deep neural network accelerators. The second paper aims at solving the time-consuming problem in optical neural networks through an acceleration method for learning the parameters of programmable Mach-Zehnder interferometers (MZIs) with a multiple-layered structure. The third paper presents a Mobileware architecture that employs a channel stationary dataflow to efficiently handle different input/weight reuse patterns and smaller number of multiplications for dot product computations in the depthwise convolutional layers, thereby improving the utilization of hardware multipliers. The last paper proposes a framework for area-efficient multi-task BERT execution on the ReRAM-based accelerator, and employs a two-stage weight compressor to shrink the decomposed models by analyzing the properties of the ReRAM-based accelerator.

O-HAS: Optical Hardware Accelerator Search for Boosting Both Acceleration Performance and Development Speed

Mengquan Li, Rice University
Zhongzhi Yu, Rice University
Yongan Zhang, Rice University
Yonggan Fu, Rice University
Yingyan Lin, Rice University

Acceleration method for learning fine-layered optical neural networks

Kazuo Aoyama, NTT Communication Science Laboratories
Hiroshi Sawada, NTT Communication Science Laboratories

Mobileware: A High-Performance MobileNet Accelerator with Channel Stationary Dataflow

Sungju Ryu, Pohang University of Science and Technology
Youngtaek Oh, Pohang University of Science and Technology
Jae-Joon Kim, Postech

A Framework for Area-efficient Multi-task BERT Execution on ReRAM-based Accelerators

Myeonggu Kang, Korea Advanced Institute of Science and Technology
Hyein Shin, Korea Advanced Institute of Science and Technology
Jaekang Shin, Korea Advanced Institute of Science and Technology
Lee-Sup Kim, Korea Advanced Institute of Science and Technology

4B – RESILIENT AND EFFICIENT EMBEDDED APPLICATIONS

Time: 7:20 AM – 8:00 AM

Moderator: Leonidas Kosmidis, Barcelona Supercomputing Center

This session includes four papers that aim at building resilient and efficient embedded systems with novel methods, including a hybrid strategy with multiple Time-triggered queues to achieve robust Time-sensitive networking, a hash-signature-based approach to enable high-accuracy detection of fault-injection attacks on deep neural networks, an adaptive object model to jointly optimize energy and detection efficiency by exploiting the spatial co-occurrence probability of object categories, and a high-performance accelerator for super-resolution model LAPAR on embedded GPUs.

Robust Time-Sensitive Networking with Delay Bound Analyses

Guoqi Xie, Hunan University

Xiangzhen Xiao, Hunan University

Hong Liu, Shanghai Trusted Industrial Control Platform Co., Ltd.

Li Renfa, Hunan University

Wanli Chang, University of York

HASHTAG: Hash Signatures for Online Detection of Fault-Injection Attacks on Deep Neural Networks

Mojan Javaheripi, University of California San Diego

Farinaz Koushanfar, University of California San Diego

A High-Performance Accelerator for Super-Resolution Processing on Embedded GPU

Wenqian Zhao, The Chinese University of Hong Kong

Qi Sun, The Chinese University of Hong Kong

Yang Bai, The Chinese University of Hong Kong

Haisheng Zheng, SmartMore

Wenbo Li, The Chinese University of Hong Kong

Bei Yu, The Chinese University of Hong Kong

Martin Wong, The Chinese University of Hong Kong

AdaCon: Adaptive Context-Aware Object Detection for Resource-Constrained Embedded Devices

Marina Neseem, Brown University

Sherief Reda, Brown University

4C – SIMULATION AND TEST GENERATION TOOLS

Time: 7:20 AM – 8:00 AM

Moderator: Abhijit Chatterjee, Georgia Tech

Research on advanced simulation and test generation algorithms is presented. The first paper advances logic simulation on GPUs via gate level parallelism. The second paper discusses how architectural level state variables can be determined that allow co-verification of hardware with software and firmware. The third paper presents a novel methodology for machine learning based test pattern generation for neuromorphic ICs. The fourth paper presents an instruction-accurate RISV-V multi-core simulator that can simulate systems with thousands of cores.

Accelerate Logic Re-simulation on GPU via Gate/Event Parallelism and State Compression

Cheng Zeng, Fudan University

Fan Yang, Fudan University

Xuan Zeng, Fudan University

Generating Architecture-Level Abstractions from RTL Designs for Processors and Accelerators, Part I: Determining Architectural State Variables

Yu Zeng, Princeton University

Bo-Yuan Huang, Princeton University

Hongce Zhang, Princeton University

Aarti Gupta, Princeton University

Sharad Malik, Princeton University

Machine Learning-Based Test Pattern Generation for Neuromorphic Chips

Hsiao-Yin Tseng, Graduate Institute of Electronics Engineering, National Taiwan University

I-Wei Chiu, Graduate Institute of Electronics Engineering, National Taiwan University

Mu-Ting Wu, Graduate Institute of Electronics Engineering, National Taiwan University

Chien-Mo Li, Graduate Institute of Electronics Engineering, National Taiwan University

Banshee: A Fast LLVM-Based RISC-V Binary Translator

Samuel Riedel, ETH Zürich

Fabian Schuiki, ETH Zürich

Paul Scheffler, Integrated Systems Laboratory, ETH Zurich

Florian Zaruba, ETH Zürich

Luca Benini, Università di Bologna and ETH Zurich

SPECIAL SESSION 4D – VLSI FOR 5G AND BEYOND WIRELESS IN THE AI ERA: ALGORITHM, HARDWARE AND SYSTEM

Time: 7:20 AM – 8:00 AM

Moderator: Jiang Hu, Texas A&M University

The state-of-the-art AI techniques, which have demonstrated the unprecedented success in many fields, are also beginning to reshape the landscape of telecommunication. However, drastically different from other AI-powered applications, modern wireless communication has very strict specifications on transmission accuracy and processing speed, while meanwhile the currently powerful AI approaches, such as deep neural networks, are inherently computation intensive and storage intensive. Therefore, severe challenges, together with the exciting opportunities, are posed and raised for both AI and VLSI communities towards enabling the next-generation wireless systems.

At this special intersection among wireless, AI and VLSI, recently researchers with different background have made significant progress in addressing the above challenges. This special session will present these cross-layer (algorithm to hardware to system) and cross-domain (digital to analog to RF) research efforts to provide inspiring solutions and insights.

FedSwap: A Federated Learning based 5G Decentralized Dynamic Spectrum Access System *(Invited Paper)*

Zhihui Gao, Duke University

Ang Li, Duke University

Yunfan Gao, ETH Zürich

Bing Li, Capital Normal University

Yu Wang, Tsinghua University

Yiran Chen, Duke University

A Hybrid FPGA-ASIC Delayed Feedback Reservoir System to Enable Spectrum Sensing/Sharing for Low Power IoT Devices *(Invited Paper)*

Osaze Shears, Virginia Polytechnic Institute and State University

Kangjun Bai, Virginia Polytechnic Institute and State University

Lingjia Liu, Virginia Polytechnic Institute and State University

Yang Cindy Yi, Virginia Polytechnic Institute and State University

Algorithm and Hardware Co-design for Deep Learning-powered Channel Decoder: A Case Study *(Invited Paper)*

Boyang Zhang, Rutgers University

Yang Sui, Rutgers University

Lingyi Huang, Rutgers University

Siyu Liao, Amazon

Chunhua Deng, ScaleFlux

Bo Yuan, Rutgers University

5G and Beyond Wireless in AI Era: ML-Driven Performance-Adaptive Terahertz Transceivers

Payam Heydari, University of California, Irvine

5A – HARDWARE SOFTWARE CO-DESIGN FOR ADVANCED DEEP NEURAL NETWORKS

Time: 9:00 AM – 9:45 AM

Moderator: Lilas M Alrahis, New York University Abu Dhabi

This session presents different methods for hardware software co-design of advances DNNs. The first paper presents a convergence monitoring method to resolve the redundancy in massive training iterations when targeting the transfer learning-based task adaptation of on-device training workloads. The second paper presents a resource-aware scheduling framework for efficient multi-tenant DNN inference on GPUs that automatically coordinates DNN computing in different execution levels. The third paper presents a tensor program generation system AutoGTCO), which explores the optimization of operator fusion in the transformer model, for vision tasks on GPUS, through a novel dynamic programming algorithm. The fourth paper presents a GNN and accelerator co-search framework to automatically search for the matched GNN structures and accelerators to maximize both task accuracy and acceleration efficiency.

A Convergence Monitoring Method for DNN Training of On-Device Task Adaptation

Seungkyu Choi, Korea Advanced Institute of Science and Technology
Jaekang Shin, Korea Advanced Institute of Science and Technology
Lee-Sup Kim, Korea Advanced Institute of Science and Technology

Automated RunTime-Aware Scheduling for Multi-Tenant DNN Inference on GPU

Fuxun Yu, George Mason University
Shawn Bray, University of Maryland, Baltimore County
Di Wang, Microsoft
Longfei Shangguan, Microsoft
Xulong Tang, University of Pittsburgh
Chenchen Liu, University of Maryland, Baltimore County
Xiang Chen, George Mason University

AutoGTCO: Graph and Tensor Co-Optimize for Image Recognition with Transformers on GPU

Yang Bai, The Chinese University of Hong Kong
Xufeng Yao, The Chinese University of Hong Kong
Qi Sun, The Chinese University of Hong Kong
Bei Yu, The Chinese University of Hong Kong

G-CoS: GNN-Accelerator Co-Search Towards Both Better Accuracy and Efficiency

Yongan Zhang, Rice University
Haoran You, Rice University
Yonggan Fu, Rice University
Tong Geng, Pacific Northwest National Laboratory

Ang Li, Pacific Northwest National Laboratory
Yingyan Lin, Rice University

5B – SECURITY OF ML SYSTEMS

Time: 9:00 AM – 9:45 AM

Moderator: Benjamin Tan, New York University

The advancement of AI accelerators has seen the rise of novel and complex attacks on these systems to extract training data or to corrupt the inference. AI models have also been used to attack the supply-chain to extract design details. This session explores interesting attacks that steal the ML models through the scan-chain, or through a cold boot attack. The session also explores using AI models for performing reverse-engineering attacks. The session will also present an interesting countermeasure that protects ML systems against Noise and Bit-Flipping attacks.

Hyperdimensional Self-Learning Systems Robust to Technology Noise and Bit-Flip Attacks

Prathyush Poduval, University of California Irvine

Yang Ni, University of California Irvine

Kai Ni, Rochester Institute of Technology

Yeseong Kim, Daegu Gyeongbuk Institute of Science and Technology

Raghavan Kumar, Intel Labs

Rosario Cammarota, Intel Labs

Mohsen Imani, University of California Irvine

GPU Overdrive Fault Attacks on Neural Networks

Majid Sabbagh, Northeastern University

Yunsi Fei, Northeastern University

David Kaeli, Northeastern University

Stealing Neural Network Models through the Scan Chain: A New Threat for ML Hardware

Seetal Potluri, North Carolina State University

Aydin Aysu, North Carolina State University

DeepFreeze: Cold Boot Attack and Model Recovery on Commercial EdgeML Device *(BPA award nominee)*

Yoo-Seung Won, Temasek Laboratories, Nanyang Technological University

Soham Chatterjee, Nanyang Technological University

Dirmanto Jap, Temasek Laboratories, Nanyang Technological University

Shivam Bhasin, Temasek Laboratories, Nanyang Technological University

Arindam Basu, Nanyang Technological University

5C – MANAGING COMPLEXITY WITH CELL DESIGN AND PARTITIONING

Time: 9:00 AM – 9:45 AM

Moderator: Patrick H. Madden, SUNY Binghamton University

VLSI circuits pose design problems of ever increasing size; managing complexity has been essential to the success of Moore's Law. In this session, the four papers focus on making design problems tractable without sacrificing quality. The first paper presents new algorithmic techniques for cell layout, utilizing a globally optimal search tree to handle transistor folding. The second explores ambipolar reconfigurable gates, which can lead to reductions in both area and static power consumption. The third paper presents advances in spectral methods for hypergraph clustering and partitioning, leveraging recent work from the AI and machine learning communities. The final paper uses topology-driven partitioning to manage the complexity of multi-FPGA systems.

Simultaneous Transistor Folding and Placement in Standard Cell Layout Synthesis

Kyeonghyeon Baek, Seoul National University

Taewhan Kim, Seoul National University

Exploring Physical Synthesis for Circuits based on Emerging Reconfigurable Nanotechnologies

Andreas Krinke, Technische Universität Dresden

Shubham Rai, Technische Universität Dresden

Akash Kumar, Technische Universität Dresden

Jens Lienig, Technische Universität Dresden

HyperSF: Spectral Hypergraph Coarsening via Flow-based Local Clustering

Ali Aghdaei, Stevens Institute of Technology

Zhiqiang Zhao, Stevens Institute of Technology

Zhuo Feng, Stevens Institute of Technology

TopoPart: a Multi-level Topology-Driven Partitioning Framework for Multi-FPGA Systems

Dan Zheng, The Chinese University of Hong Kong

Xinshi Zang, The Chinese University of Hong Kong

Martin Wong, The Chinese University of Hong Kong

SESSION 5D | TUTORIAL: HARDWARE AWARE LEARNING FOR MEDICINE

Time: 9:00 AM – 9:45 AM

Moderator: Zhezhi He, Shanghai Jiaotong University

Imaging technologies and drug development are two critical tasks in the healthcare industry. In the recent Critical Path initiative, US Food and Drug Administration (FDA) has joined the National Cancer Institute (NCI), the pharmaceutical industry, and academia in a number of activities that will facilitate the use of medical imaging during drug discovery. In this session, we will present four talks from collaborations between academic and health providers that demonstrate how automated machine learning can facilitate various clinical problems from biomarker analysis, disease diagnosis to drug discovery. They demonstrate various problems where electronic design automation community can contribute to the development of new therapies to treat disease.

Contrastive Learning with Temporal Correlated Medical Images: A Case Study using Lung Segmentation in Chest X-Rays *(Invited Paper)*

Dewen Zeng, University of Notre Dame

John N Kheir, Boston Children's Hospital/Harvard Medical School

Peng Zeng, Boston Children's Hospital

Yiyu Shi, University of Notre Dame

Federated Contrastive Learning for Dermatological Disease Diagnosis via On-device Learning *(Invited Paper)*

Yawen Wu, University of Pittsburgh

Dewen Zeng, University of Notre Dame

Zhepang Wang, George Mason University

Yi Sheng, George Mason University

Lei Yang, University of New Mexico

Alaina J James, University of Pittsburgh Medical Center

Yiyu Shi, University of Notre Dame

Jingtong Hu, University of Pittsburgh

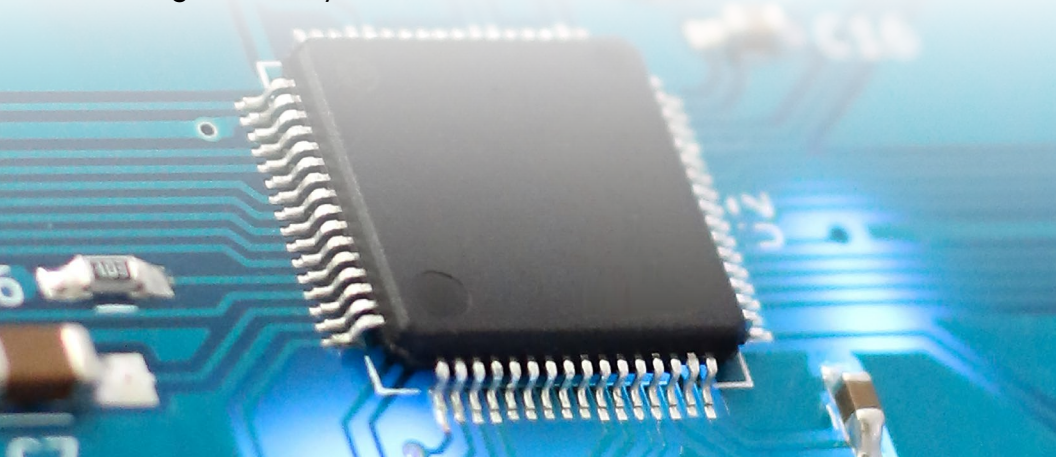
SESSION 5D | TUTORIAL: HARDWARE AWARE LEARNING FOR MEDICINE (CONT.)

Optimizing FPGA-based Accelerator Design for Large-Scale Molecular Similarity Search *(Invited Paper)*

Hongwu Peng, University of Connecticut
Shiyang Chen, Stevens Institute of Technology
Zhepeng Wang, George Mason University
Junhuan Yang, University of New Mexico
Scott Weitze, Stevens Institute of Technology
Tong Geng, Pacific Northwest National Laboratory
Ang Li, Pacific Northwest National Laboratory
Jinbo Bi, University of Connecticut
Minghu Song, University of Connecticut
Weiwen Jiang, George Mason University
Hang Liu, Stevens Institute of Technology
Caiwen Ding, University of Connecticut

FL-DISCO: Federated Generative Adversarial Network for Graph-based Molecule Drug Discovery *(Invited Paper)*

Daniel Manu, University of New Mexico
Yi Sheng, George Mason University
Junhuan Yang, University of New Mexico
Jieren Deng, University of Connecticut
Tong Geng, Pacific Northwest National Laboratory
Ang Li, Pacific Northwest National Laboratory
Caiwen Ding, University of Connecticut
Weiwen Jiang, George Mason University
Lei Yang, University of New Mexico



6A – BRAIN-INSPIRED COMPUTING AND MICROFLUIDIC BIO-CHIPS

Time: 9:45 AM – 10:30 AM

Moderator: Mohamed Ibrahim, University of California, Berkeley

Driven by a biological perspective, the session brings together latest developments in two next-generation computing paradigms – brain-inspired computing and micro-fluidic bio-chips. The technical papers include pathways toward practical realization of neuromorphic systems exhibiting fault-tolerance and error resiliency. On the microfluidics side, innovative CAD techniques are proposed for high level synthesis of microfluidic bio-chip systems.

ReSpawn: Energy-Efficient Fault-Tolerance for Spiking Neural Networks considering Unreliable Memories

Rachmad Vidya Wicaksana Putra, Technische Universität Wien
Muhammad Abdullah Hanif, Technische Universität Wien
Muhammad Shafique, New York University Abu Dhabi

Binarized SNNs: Efficient and Error-Resilient Spiking Neural Networks through Binarization

Ming-Liang Wei, National Taiwan University
Mikail Yayla, TU Dortmund
Shu-Yin Ho, Macronix
Jian-Jia Chen, TU Dortmund
Chia-Lin Yang, National Taiwan University
Hussam Amrouch, University of Stuttgart

BigIntegr: One-Pass Architectural Synthesis for Continuous-Flow Microfluidic Lab-on-a-Chip Systems

Xing Huang, Technical University of Munich
Youlin Pan, Fuzhou University
Zhen Chen, Fuzhou University
Wenzhong Guo, Fuzhou University
Robert Wille, Johannes Kepler University Linz
Tsung-Yi Ho, National Tsing Hua University
Ulf Schlichtmann, Technical University of Munich

Relative-Scheduling-Based High-Level Synthesis for Flow-Based Microfluidic Biochips

Fangda Zuo, Technical University of Munich
Mengchu Li, Technical University of Munich
Tsun-Ming Tseng, Technical University of Munich
Tsung-Yi Ho, National Tsing Hua University
Ulf Schlichtmann, Technical University of Munich

6B – NEW TECHNIQUES IN TIMING AND POWER ANALYSIS

Time: 9:45 AM – 10:30 AM

Moderator: Siddhartha Nath, NVIDIA

The session explores novel techniques to improve timing, power grid design, and circuit analysis. The first paper leverages machine learning to make power grid benchmarks available to the EDA community. The second paper uses advanced optimization algorithms to tune design flow parameters. The last two papers apply novel GPUs algorithms to accelerate important timing tasks.

BeGAN: Power Grid Benchmark Generation Using a Process-portable GAN-based Methodology

Vidya A. Chhabria, University of Minnesota

Kishor Kunal, University of Minnesota

Masoud Zabihi, University of Minnesota

Sachin S. Sapatnekar, University of Minnesota

FlowTuner: A Multi-Stage EDA Flow Tuner Exploiting Parameter Knowledge Transfer

Rongjian Liang, Texas A&M University

Jinwook Jung, IBM Research

Hua Xiang, IBM Research

Lakshmi Reddy, IBM Research

Alexey Lvov, IBM Corp.

Jiang Hu, Texas A&M University

Gi-Joon Nam, IBM Research

HeteroCPR: Accelerating Common Path Pessimism Removal with Heterogeneous CPU-GPU Parallelism

Zizheng Guo, Peking University

Tsung-Wei Huang, University of Utah

Yibo Lin, Peking University

GPU-accelerated Critical Path Generation with Path Constraints

Guannan Guo, University of Illinois at Urbana-Champaign

Tsung-Wei Huang, University of Utah

Yibo Lin, Peking University

Martin Wong, The Chinese University of Hong Kong

6C – MACHINE LEARNING METHODS FOR DFM

Time: 9:45 AM – 10:30 AM

Moderator: Jhih-Rong Gao, Flex Logix

DFM applications have led the way in the application of machine learning (ML) methods in EDA, and this session presents the newest research on this topic. The first paper presents an OPC method using DNNs, introducing a new curvature term into the level set algorithm that meshes well with GPU acceleration. The second paper uses enhanced ML methods based on multi-head attention to perform hotspot labeling and localization for improved accuracy. Next a layout pattern analysis method is proposed for fault diagnosis using contrastive learning for data augmentation. Finally, the session ends with a presentation on improving wafer failure pattern classification using few-shot learning and self-supervised learning.

DevelSet: Deep Neural Level Set for Instant Mask optimization

Guojin Chen, The Chinese University of Hong Kong
Ziyang Yu, The Chinese University of Hong Kong
Hongduo Liu, The Chinese University of Hong Kong
Yuzhe Ma, The Chinese University of Hong Kong
Bei Yu, The Chinese University of Hong Kong

Hotspot Detection via Multi-task Learning and Transformer Encoder

Binwu Zhu, The Chinese University of Hong Kong
Ran Chen, The Chinese University of Hong Kong
Xinyun Zhang, SmartMore
Fan Yang, Fudan University
Xuan Zeng, Fudan University
Bei Yu, The Chinese University of Hong Kong
Martin Wong, The Chinese University of Hong Kong

A Unified Framework for Layout Pattern Analysis with Deep Causal Estimation

Ran Chen, The Chinese University of Hong Kong
Shoubo Hu, Huawei Noah's Ark Lab
Zhitang Chen, Huawei Noah's Ark Lab
Shengyu Zhu, Huawei Noah's Ark Lab
Bei Yu, The Chinese University of Hong Kong
Pengyun Li, HiSilicon
Cheng Chen, HiSilicon
Yu Huang, Mentor, A Siemens Business
Jianye Hao, Huawei Noah's Ark Lab

When Wafer Failure Pattern Classification Meets Few-shot Learning and Self-Supervised Learning

Hao Geng, The Chinese University of Hong Kong
Fan Yang, Fudan University
Xuan Zeng, Fudan University
Bei Yu, The Chinese University of Hong Kong

6D – TUTORIAL: FERROELECTRIC FET TECHNOLOGIES AND ITS APPLICATIONS: FROM DEVICE TO SYSTEM

Time: 9:45 AM – 10:30 AM

Moderator: Xunzhao Yin, Zhejiang University, **Cheng Zhuo**, Zhejiang University

The rapidly increasing volume and complexity of data is demanding the relentless scaling of computing power. With the transistor feature size approaching the physical limit, the benefits for CMOS moving forward are actually suffering from the diminishing returns. For the future energy efficient computing system, researchers have been exploiting various emerging nanotechnologies to replace the conventional CMOS technology. In particular, ferroelectric FET (FeFET) appears to be a promising candidate to continue improving energy efficiency for data-intensive applications. Especially the advances in scalability and compatibility in FeFET have sparked growing interest in FeFET from device, circuit to system implementation. Recently, fueled by the new application fields (e.g., in memory computing, neuromorphic computing, etc.) and the continuous successes in technology development, FeFET has seen an outburst of research activities. Many researchers and developers are cautiously optimistic about its future. Thus, we would like to invite the experts in the field to give a tutorial on FeFET, its recent technology advances, challenges, and opportunities, with particular emphasis upon device modeling, circuit design, and system optimization. This tutorial will start with an overview of FeFET. Then it will review the working principles, technology options, and reliability issues for FeFET. After that, a few state-of-the-art solutions for circuit and system leveraging the unique properties of FeFET will be presented. We will conclude the tutorial on a brief outlook for FeFET's future.

Ferroelectric FET Technology and Applications: From Devices to Systems – Overview

Cheng Zhuo, Zhejiang University

Ferroelectric FET Technology and Applications: From Devices to Systems – Device Modeling

Kai Ni, Rochester Institute of Technology

Ferroelectric FET Technology and Applications: From Devices to Systems – Device-Circuit Co-Optimization

Hussam Amrouch, University of Stuttgart

Ferroelectric FET Technology and Applications: From Devices to Systems – Cross-Layer Evaluation

Xiaobo Sharon Hu, University of Notre Dame

7A – IN-MEMORY COMPUTING CIRCUITS AND ARCHITECTURES

Time: 10:30 AM – 11:00 AM

Moderator: Marc Riedel, University of Minnesota, Twin Cities

The session showcases latest developments in In-Memory Computing to overcome the von-Neumann bottleneck in machine learning workloads. The technical papers consider innovations at the circuit and architecture level to optimize peripheral overhead along with novel hybridized analog-digital computing schemes.

Quarry: Quantization-based ADC Reduction for ReRAM-based Deep Neural Network Accelerators

Azat Azamat, Ulsan National Institute of Science and Technology
Faiz Asim, Ulsan National Institute of Science and Technology
Jong Eun Lee, Ulsan National Institute of Science and Technology

Peripheral Circuitry Assisted Mapping Framework for Resistive Logic-In-Memory Computing

Shuhang Zhang, Technical University of Munich
Hai (Helen) Li, Duke University
Ulf Schlichtmann, Technical University of Munich

Hybrid Analog-Digital In-Memory Computing

Muhammad Rashedul Haq Rashed, University of Central Florida
Sumit Kumar Jha, University of Texas at San Antonio
Rickard Ewetz, University of Central Florida



Unsplash, Jan Antonin Kolar

7B – TECHNIQUES TOWARDS FULLY AUTOMATED ANALOG IC DESIGNS

Time: 10:30 AM – 11:00 AM

Moderator: Nuno Horta, Instituto Superior Tecnico, University of Lisbon

Analog IC design automation has long been an unsolved challenge. This session highlights the latest progress towards solving this challenge. The first paper introduces a reinforcement learning approach for automatic topology synthesis, the most difficult part of analog design automation, for power converters. The second paper utilizes low-cost schematic simulation and maps it to post-layout models via transfer learning, subsequently achieving effective layout-aware device sizing. Last but not the least, OpenSAR is a demonstration of automated design flow at the analog system level.

From Specification to Topology: Automatic Power Converter Design via Reinforcement Learning

Shaoze Fan, New Jersey Institute of Technology

Ningyuan Cao, Georgia Institute of Technology

Shun Zhang, New Jersey Institute of Technology, IBM

Jing Li, New Jersey Institute of Technology

Xiaoxiao Guo, IBM Research

Xin Zhang, IBM Research

From Specification to Silicon: Towards Analog/Mixed-Signal Design Automation using Surrogate NN Models with Transfer Learning

Juzheng Liu, University of Southern California

Shiyu Su, University of Southern California

Meghna Madhusudan, University of Minnesota

Mohsen Hassanpourghadi, University of Southern California

Samuel Saunders, University of Southern California

Qiaochu Zhang, University of Southern California

Rezwan Rasul, University of Southern California

Yaguang Li, Texas A&M University

Jiang Hu, Texas A&M University

Arvind Kumar Sharma, University of Minnesota

Sachin S. Sapatnekar, University of Minnesota

Ramesh Harjani, University of Minnesota

Anthony Levi, University of Southern California

Sandeep Gupta, University of Southern California

Mike Chen, University of Southern California

OpenSAR: An Open Source Automated End-to-end SAR ADC Compiler

Mingjie Liu, University of Texas Austin

Xiyuan Tang, University of Texas at Austin

Keren Zhu, University of Texas at Austin

Hao Chen, University of Texas at Austin

Nan Sun, University of Texas at Austin

David Z. Pan, University of Texas at Austin

SPECIAL SESSION 7C – BIG DATA, BIG DEAL: DATA ANALYSIS AND SMART TUNING OF EDA FLOWS

Time: 10:30 AM – 11:00 AM

Moderator: Iris Hui-Ru, National Taiwan University, Gi-Joon Nam, IBM Research

Deployment of systematic, standardized metrics collection and machine learning from big data has turned the corner in the past year. Industrial and academic efforts have put forward standardized metrics APIs and numerous proofs of value from ML based on big data. At the same time, production design methodologies and EDA vendor offerings have achieved substantial runtime and QOR improvements using reinforcement learning, recommender systems and other ML frameworks. This session gives updates on how big data has become a big deal in the tuning of design tools and flows -- from academic, fabless, IDM and EDA perspectives.

The first talk will describe a standard enablement of design and flow metrics collection, along with automated tool/flow tuning for PPA, developed as an initiative of the IEEE CEDA Design Automation Technical Committee. The second talk will present two machine learning-based enhancements of PPA optimization, including transfer learning to find an optimal point and required place-and-route tool parameters, and an evolutionary algorithm to achieve a Pareto-optimal PPA outcome for an unseen design. The third talk will describe methods used for tuning of an industrial design flow, where online and offline machine learning techniques work holistically together; challenges and potential research directions are also presented. The session will close with connections to the intense recent interest in deep reinforcement learning (RL). The speakers will present the use of RL for improvement of PPA and turnaround time within a commercial physical synthesis flow, across applications ranging from gate sizing to the broader DSO.ai platform.

METRICS2.1 and Flow Tuning in the IEEE CEDA Robust Design Flow and OpenROAD *(Invited Paper)*

Jinwook Jung, IBM Research

Andrew B. Kahng, University of California San Diego

Seungwon Kim, University of California San Diego

Ravi Varadarajan, University of California San Diego

Fast and Accurate PPA Modeling with Transfer Learning *(Invited Paper)*

Paul Franzon, North Carolina State University

W. Rhett Davis, North Carolina State University

Rajeev Jain, Qualcomm

Luis Francisco, Synopsys

Billy Huggins, Synopsys

Online and Offline Machine Learning for Industrial Design Flow Tuning *(Invited Paper)*

Matthew Ziegler, IBM Research

Jihye Kwon, Columbia University

Hung-Yi Liu, Intel

Luca P. Carloni, Columbia University

Reinforcement Learning-Driven Optimization for Superior Performance, Power and Productivity

Thomas Andersen, Synopsys

Siddhartha Nath, NVIDIA

7D – TUTORIAL: A QUANTUM MACHINE LEARNING CO-DESIGN FRAMEWORK TOWARDS QUANTUM ADVANTAGE

Time: 10:30 AM – 11:00 AM

Moderator: Rudy Raymond, IBM Research, Weiwen Jiang, George Mason University

Recent advances in quantum computing greatly encourage researchers to design quantum algorithms for different applications and explore the potential of accelerating those applications using quantum computing. With a wide range of applications, machine learning (ML) is one of the most promising algorithms to be accelerated by quantum computing, because (1) ML on classical computing gradually meets performance bottlenecks when the neural network grows wide and deep, (2) quantum computing can provide incomparable computing power over classical computing, and (3) the fundamentals of ML and quantum computing are tensor operations. However, in the near-term future, the quantum computer still has great constraints, which is widely known as noisy intermediate-scale quantum (NISQ). To enable quantum machine learning in the NISQ era, there are two questions needing to be answered: how to optimize the quantum algorithm for machine learning tasks, and how to map the quantum algorithms to the physical qubits with high noise levels and limited scale. Toward the goal of making impacts on quantum computing and quantum ML in the NISQ era, this tutorial/special session focuses on exploring the best quantum algorithm for ML tasks and mapping quantum algorithms to physical qubits with high noise levels. The session consists of three presentations: the first talk will provide a tutorial on utilizing the state-of-the-art quantum neural networks, including Variational Quantum Circuit and QuantumFlow, to explore quantum neural architectures, and then, the second presentation will introduce a general-purpose qubit mapping approach for depth and gate count minimization to improve the fidelity of the applications in NISQ era. Last, an application-specific compiler will be presented to co-optimize the neural network model and quantum circuit implementation, such that the identified network model can be resilient to the noise existing in the physic qubits.

7D – TUTORIAL: A QUANTUM MACHINE LEARNING CO-DESIGN FRAMEWORK TOWARDS QUANTUM ADVANTAGE (CONT.)

Exploration of Quantum Neural Architecture by Mixing Quantum Neuron Designs *(Invited Paper)*

Zhepeng Wang, George Mason University
Zhiding Liang, University of Notre Dame
Shanglin Zhou, University of Connecticut
Caiwen Ding, University of Connecticut
Jinjun Xiong, University at Buffalo
Yiyu Shi, University of Notre Dame
Weiwen Jiang, George Mason University

Optimal Qubit Mapping with Simultaneous Gate Absorption *(Invited Paper)*

Bochen Tan, University of California, Los Angeles
Jason Cong, University of California, Los Angeles

Can Noise on Qubits Be Learned in Quantum Neural Network? A Case Study on QuantumFlow *(Invited Paper)*

Zhiding Liang, University of Notre Dame
Zhepeng Wang, George Mason University
Junhuan Yang, University of New Mexico
Lei Yang, University of New Mexico
Jinjun Xiong, University at Buffalo
Yiyu Shi, University of Notre Dame
Weiwen Jiang, George Mason University

CADENCE SPONSOR SESSION

Time: 11:00 AM – 12:00 PM

Charting the Path to 3nm & More than Moore

Speaker: **Rod Metcalfe**, Cadence Design Systems

WEDNESDAY SCHEDULE

Join the ICCAD Gather Space to network and continue asking questions (for 30 minutes after each session concludes)

7:20 – 8:00AM 4:20 - 5PM CET (GERMANY), 10:20 - 11PM CST (CHINA)

8A: Acceleration methodologies for Reconfigurable Computing

8B: SoC Security

8C: Placement Techniques for Advanced VLSI Technology

Special Session 8D: Hardware/software Co-design for Neuromorphic Computing

8:00 – 9:00AM 5 - 6PM CET (GERMANY), 11PM - 12AM CST (CHINA)

Keynote: RISC-V Is Inevitable

David Patterson, University of California, Berkeley

9:00 – 9:45AM 6 - 6:45PM CET (GERMANY), 12 - 12:45AM CST (CHINA)

9A: System-Level Optimization of Machine Learning Applications Execution on Heterogeneous Computing Systems

9B: Coming to Your Chips: NVM & Optical Interconnects

9C: Clock tree synthesis, placement, and routing - how to get the best results from the backend of the flow

Special Session 9D: Brain-Inspired Computing: Adventure from Beyond CMOS Technologies to Beyond von Neumann Architectures

9:45 – 10:30AM 6:45 - 7:30PM CET (GERMANY), 12:45 - 1:30AM CST (CHINA)

10A: Pushing the Boundaries of Machine Learning and Synthesis

10B: Hardware Approaches for Embedded Performance and Robustness

10C: Advanced Design Verification Methods

Special Session 10D: Security Closure of Physical Layouts

10:30 – 11:00AM 7:30 - 8PM CET (GERMANY), 1:30 - 2AM CST (CHINA)

Special Session 11A: Harnessing the Power of Machine Learning: EDA to Accelerator Design

11B: Parallel Power Grid Solver and Geometry-Based Techniques for Analog Circuit Design

11C: Reliability: From Interconnects to Systems

Special Session 11D: 2021 CAD Contest at ICCAD

11:00 – 12:00PM 8 - 9PM CET (GERMANY), 2 - 3AM CST (CHINA)

Synopsys Sponsor Session

Mike Borza, Synopsys

8A – ACCELERATION METHODOLOGIES FOR RECONFIGURABLE COMPUTING

Time: 7:20 AM – 8:00 AM

Moderator: Sotirios Xydis, Harokopio University of Athens

This session on Reconfigurable Computing includes four papers on acceleration methodologies.

Polyhedral-based Pipelining of Imperfectly-Nested Loop for CGRAs

Dajiang Liu, Chongqing University
Ting Liu, Chongqing University
Xingyu Mo, Chongqing University
Jiaxing Shang, Chongqing University
Jiang Zhong, Chongqing University
Shouyi Yin, Tsinghua University

GraphLily: Accelerating Graph Linear Algebra on HBM-Equipped FPGAs

Yuwei Hu, Cornell University
Yixiao Du, Cornell University
Ecenur Ustun, Cornell University
Zhiru Zhang, Cornell University

Accelerating Framework of Transformer by Hardware Design and Model Compression Co-Optimization

Panjie Qi, East China Normal University
Edwin Hsing-Mean Sha, East China Normal University
Qingfeng Zhuge, East China Normal University
Hongwu Peng, University of Connecticut
Shaoyi Huang, University of Connecticut
Zhenglun Kong, Northeastern University
Yuhong Song, East China Normal University
Bingbing Li, University of Connecticut

DALTA: A Decomposition-based Approximate Lookup Table Architecture

Chang Meng, Shanghai Jiao Tong University
Zhiyuan Xiang, Shanghai Jiao Tong University
Niyiqiu Liu, Shanghai Jiao Tong University
Yixuan Hu, Peking University
Jiahao Song, Peking University
Runsheng Wang, Peking University
Ru Huang, Peking University
Weikang Qian, Shanghai Jiao Tong University

8B – SOC SECURITY

Time: 7:20 AM – 8:00 AM

Moderator: Darshana Jayasinghe, University of New South Wales

An insecure system on a chip (SoC) has catastrophic consequences. Unprotected systems are rife with timing and power side channels that leak confidential information. Unauthorized access to low level system resources can root a system. This session presents techniques to verify SoC access control systems, detect and understand timing flows, mitigate power side channel leakage, and determine important state registers.

Aker: A Design and Verification Framework for Safe and Secure SoC Access Control

Francesco Restuccia, Scuola Superiore Sant'Anna Pisa

Andres Meza, University of California, San Diego

Ryan Kastner, University of California, San Diego

Early Validation of SoCs Security Architecture Against Timing Flows Using SystemC-based VPs

Mehran Goli, University of Bremen

Rolf Drechsler, University of Bremen/DFKI GmbH

iSTELLAR: intermittent Signature aTtenuation Embedded CRYPTO with Low-Level metaI Routing

Jeremy Blackstone, University of California, San Diego

Debayan Das, Purdue University

Alric Althoff, University of California, San Diego

Shreyas Sen, ECE, Purdue University

Ryan Kastner, University of California, San Diego

ReIGNN: State Register Identification Using Graph Neural Networks for Circuit Reverse Engineering

Subhajit Dutta Chowdhury, University of Southern California

Kaixin Yang, University of Southern California

Pierluigi Nuzzo, University of Southern California

8C – PLACEMENT TECHNIQUES FOR ADVANCED VLSI TECHNOLOGY

Time: 7:20 AM – 8:00 AM

Moderator: Jinwook Jung, IBM Research

Placement is of particular importance in VLSI physical design flow. Its importance has become even more significant in recent years due to extreme advances in the VLSI process and design technologies along with the footprint scaling of standard cells. This session presents four papers tackling the challenging placement problems arising in advanced VLSI technology. The first paper proposes a routability-driven placement formulation that effectively mitigates global and local routing congestions. The second paper studies net weighting and placement regions to help analytic placers come up with better placement solutions for datapath circuits. The third paper presents non-uniform row configuration and placement for circuits utilizing non-integer multi-height cells. Finally, the last paper describes challenges in mixed-size FPGA placement and proposes a mixed-size FPGA quadratic placer supporting efficient macro placement.

Routability-driven Global Placer Target on Removing Global and Local Congestion for VLSI Designs

Jai-Ming Lin, Department of Electrical Engineering, National Cheng Kung University

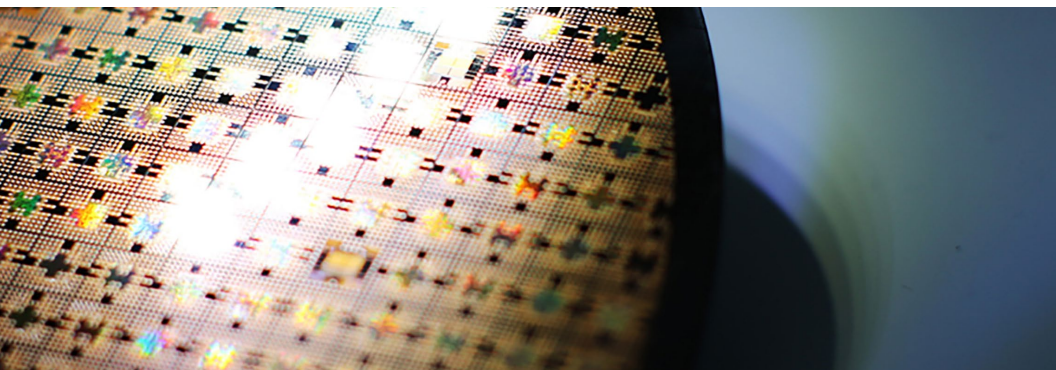
Chung-Wei Huang, Department of Electrical Engineering, National Cheng Kung University

Liang-Chi Zane, Department of Electrical Engineering, National Cheng Kung University

Min-Chia Tsai, Department of Electrical Engineering, National Cheng Kung University

Chen-Fa Tsai, Department of Physical Design Service, Global Unichip Corporation

Che-Li Lin, Department of Physical Design Service, Global Unichip Corporation



8C – PLACEMENT TECHNIQUES FOR ADVANCED VLSI TECHNOLOGY (CONT.)

DAPA: A Dataflow-aware Analytical Placement Algorithm for Modern Mixed-size Circuit Designs

Jai-Ming Lin, Department of Electrical Engineering, National Cheng Kung University

Wei-Fan Huang, Department of Electrical Engineering, National Cheng Kung University

Yao-Chieh Chen, Department of Electrical Engineering, National Cheng Kung University

Yi-Ting Wang, Department of Electrical Engineering, National Cheng Kung University

Po-Wen Wang, Department of Electrical Engineering, National Cheng Kung University

A Row-Based Algorithm for Non-Integer Multiple-Cell-Height Placement

Zih-Yao Lin, National Taiwan University

Yao-Wen Chang, National Taiwan University

AMF-Placer: High-Performance Analytical Mixed-size Placer for FPGA

Tingyuan Liang, The Hong Kong University of Science and Technology

Gengjie Chen, The Chinese University of Hong Kong

Jieru Zhao, Shanghai Jiao Tong University

Sharad Sinha, Indian Institute of Technology, Goa

Wei Zhang, The Hong Kong University of Science and Technology



Olympiagelände München, München Tourismus, Jan Saurer

SPECIAL SESSION 8D – HARDWARE/SOFTWARE CO-DESIGN FOR NEUROMORPHIC COMPUTING

Time: 7:20 AM – 8:00 AM

Moderator: Antonino Tumeo, Pacific Northwest National Laboratory,
Vito Giovanni Castellana, Pacific Northwest National Laboratory,
Marco Minutoli, Pacific Northwest National Laboratory

Neuromorphic computing platforms have shown the potential of achieving significant energy efficiency improvements for artificial intelligence and machine learning approaches with respect to the current state of the art in custom accelerators for a variety of applications, from the edge to large scale high-performance computing platforms. However, despite the recent and quick advancements on the hardware front, the hardware/software interface, and the software stack to make these platforms effectively usable and integrable remain largely unexplored. This special session will highlight the key the role of hardware/software co-design and design automation for making neuromorphic computing actually exploitable and integrable in next generation hardware design flows and complex heterogeneous system. This special session will discuss programming and usability issues of neuromorphic computing, approaches for design space exploration for neuromorphic hardware, and the opportunities provided by modern compiler-based hardware generation infrastructures for combining neuromorphic hardware and digital accelerators in complex heterogeneous systems.

Top-Down Neuromorphic Hardware Co-Design via Machine Learning and Simulation

Catherine Schuman, Oak Ridge National Laboratory

A Design Flow for Mapping Spiking Neural Networks to Many-Core Neuromorphic Hardware *(Invited Paper)*

Shihao Song, Drexel University

M. Lakshmi Varshika, Drexel University

Anup Das, Drexel University

Nagarajan Kandasamy, Drexel University

Architecture Search for Neuromorphic Design

Hai (Helen) Li, Duke University

SPECIAL SESSION 8D – HARDWARE/SOFTWARE CO-DESIGN FOR NEUROMORPHIC COMPUTING (CONT.)

Automated Generation of Integrated Digital and Spiking Neuromorphic Machine Learning Accelerators

Nicolas Bohm Agostini, Pacific Northwest National Laboratory
Northeastern University

Serena Curzel, Pacific Northwest National Laboratory Politecnico di Milano

Ismet Dagli, Pacific Northwest National Laboratory Colorado School of Mines

Shihao Song, Pacific Northwest National Laboratory Drexel University

Ankur Limaye, Pacific Northwest National Laboratory

Cheng Tan, Pacific Northwest National Laboratory

Marco Minutoli, Pacific Northwest National Laboratory

Vito Giovanni Castellana, Pacific Northwest National Laboratory

Vinay Amatya, Pacific Northwest National Laboratory

Joseph Manzano, Pacific Northwest National Laboratory

Anup Das, Drexel University

Fabrizio Ferrandi, Politecnico di Milano

Antonino Tumeo, Pacific Northwest National Laboratory



Schwabinger Tor München, München Tourismus, Tommy Lösch

9A – SYSTEM-LEVEL OPTIMIZATION OF MACHINE LEARNING APPLICATIONS EXECUTION ON HETEROGENEOUS COMPUTING SYSTEMS

Time: 9:00 AM – 9:45 AM

Moderator: Mohamed Sabry, Nanyang Technological University

In this session, new approaches for efficiently executing machine learning applications in next-generation heterogeneous computing systems. The first paper discusses the use of flexible in-memory computing engines to improve the efficiency of memory-dominated applications, and the last three papers address the topic of optimal placement of data in memory to exploit the computational capabilities of GPUs of multiple GPUs for ML applications.

Massively Parallel Big Data Classification on a Programmable Processing In-Memory Architecture

Yeseong Kim, Daegu Gyeongbuk Institute of Science and Technology
Mohsen Imani, University of California, Irvine
Saransh Gupta, University of California, San Diego
Minxuan Zhou, University of California, San Diego
Tajana Rosing, University of California, San Diego

Overcoming the Memory Hierarchy Inefficiencies in Graph Processing Applications

Jilan Lin, University of California, Santa Barbara
Shuangchen Li, University of California, Santa Barbara
Yufei Ding, University of California, Santa Barbara
Yuan Xie, University of California, Santa Barbara

Improving Inter-kernel Data Reuse With CTA-Page Coordination in GPGPU

Xuanyi Li, National University of Defense Technology
Chen Li, National University of Defense Technology
Yang Guo, National University of Defense Technology
Rachata Ausavarungnirun, King Mongkut's University of Technology North Bangkok

ScaleDNN: Data Movement Aware DNN Training on Multi-GPU

Weizheng Xu, University of Pittsburgh
Ashutosh Pattnaik, Penn State University
Geng Yuan, Northeastern University
Yanzhi Wang, Northeastern University
Youtao Zhang, University of Pittsburgh
Xulong Tang, University of Pittsburgh

9B – COMING TO YOUR CHIPS: NVM & OPTICAL INTERCONNECTS

Time: 9:00 AM – 9:45 AM

Moderator: Dharanidhar Dang, University of California San Diego

This session brings to you two emerging paradigms, namely, NVM and optical interconnects. First, it looks into a tool for mapping both analog and digital circuitry to a ReRAM processing-in-memory module, and next, dives into making NVMs more secure by encryption. Then, we shift gears to optical interconnect with a very timely CAD simulator for flexibly designing optical NoCs, and next, a novel energy-management scheme for Optical NoC.

SSR: A Skeleton-based Synthesis Flow for Hybrid Processing-in-RRAM Modes

Feng Wang, Peking University
Guangyu Sun, Peking University
Guojie Luo, Peking University

MORE2: Morphable Encryption and Encoding for Secure NVM

Wei Zhao, Huazhong University of Science and Technology
Dan Feng, Huazhong University of Science and Technology
Yu Hua, Huazhong University of Science and Technology
Wei Tong, Huazhong University of Science and Technology
Jingning Liu, Huazhong University of Science and Technology
Jie Xu, Huazhong University of Science and Technology
Chunyan Li, Huazhong University of Science and Technology
Gaoxiang Xu, Huazhong University of Science and Technology
Yiran Chen, Duke University

ToPro: A Topology Projector and Waveguide Router for Wavelength-Routed Optical Networks-on-Chip

Zhidan Zheng, Technical University of Munich
Mengchu Li, Technical University of Munich
Tsun-Ming Tseng, Technical University of Munich
Ulf Schlichtmann, Technical University of Munich

Traffic-Adaptive Power Reconfiguration for Energy-Efficient and Energy-Proportional Optical Interconnects

Yuyang Wang, University of California, Santa Barbara
Kwang-Ting Cheng, Hong Kong University of Science and Technology

9C – CLOCK TREE SYNTHESIS, PLACEMENT, AND ROUTING – HOW TO GET THE BEST RESULTS FROM THE BACKEND OF THE FLOW

Time: 9:00 AM – 9:45 AM

Session Chair: Nima Karimpour, Xilinx

The first paper presents a place-and-route co-optimization engine. To incrementally optimize the routed wire length, cells are moved and broken nets are reconnected by A-based partial rerouting. The second paper considers on-chip variation (OCV) during clock tree synthesis, with a top-down clock tree construction approach, analyzing OCV for different possible uniform and non-uniform H-trees. The third paper proposes using neural architecture search to automatically create artificial neural networks to predict nets with design rule violations and to locate such hotspots. The fourth paper details machine learning models to predict when the sign-off results will be poor after placement, clock tree synthesis (CTS), and optimization.

Starfish: An Efficient P&R Co-Optimization Engine with A-based Partial Rerouting

Fangzhou Wang, The Chinese University of Hong Kong

Lixin Liu, The Chinese University of Hong Kong

Jingsong Chen, The Chinese University of Hong Kong

Jinwei Liu, The Chinese University of Hong Kong

Xinshi Zang, The Chinese University of Hong Kong

Martin Wong, The Chinese University of Hong Kong

An OCV-Aware Clock Tree Synthesis Methodology

Necati Uysal, University of Central Florida

Rickard Ewetz, University of Central Florida

Automatic Routability Predictor Development Using Neural Architecture Search

Chen-Chia Chang, Duke University

Jingyu Pan, Duke University

Tunhou Zhang, Duke University

Zhiyao Xie, Duke University

Jiang Hu, Texas A&M University

Weiyl Qi, Cadence Design Systems

Chung-Wei Lin, National Taiwan University

Ronjian Liang, Texas A&M University

Joydeep Mitra, Cadence Design Systems

Elias Fallon, Cadence Design Systems

Yiran Chen, Duke University

Doomed Run Prediction in Physical Design by Exploiting Sequential Flow and Graph Learning

Yi-Chen Lu, Georgia Institute of Technology

Siddhartha Nath, NVIDIA

Vishal Khandelwal, Synopsys Inc.

Sung Kyu Lim, Georgia Tech

SPECIAL SESSION 9D – BRAIN-INSPIRED COMPUTING: ADVENTURE FROM BEYOND CMOS TECHNOLOGIES TO BEYOND VON NEUMANN ARCHITECTURES

Time: 9:00 AM – 9:45 AM

Moderator: Jian-Jia Chen, TU Dortmund

The goal of this special session is to introduce and discuss different emerging technologies and how they may reshape the future of Artificial Intelligent (AI). This special session aims at providing a comprehensive overview on the latest advances in Brain-Inspired Computing. Unconventional (beyond CMOS) device technologies together with unconventional (beyond von Neumann) computing paradigms are brought together towards demonstrating how brain-inspired computing can be realized. Several concepts inspired from nature such as Logic-in-Memory (LIM), Processing-in-Memory (PIM), and Spiking Neural Networks (SNNs) are presented. Latest trends in brain-inspired computing are summarized into algorithm, technology, and application-driven innovations towards comparing different PIM architectures.

Realizing Brain-Inspired Computing with Emerging Ferroelectric Transistors

Hussam Amrouch, University of Stuttgart

Jian-Jia Chen, TU Dortmund

Mikail Yayla, TU Dortmund

Brain-Inspired Computing with Phase-Change Photonic Devices: Opportunities and Challenges

Kaushik Roy, Purdue University

Indranil Chakraborty, Purdue University

Cheng Wang, Purdue University

Brain-Inspired Computing: Algorithm, Technology, and Application- Driven Innovations

Yuan Xie, University of California, Santa Barbara

Fengbin Tu, University of California, Santa Barbara

Wenqin Huangfu, University of California, Santa Barbara

Ling Liang, University of California, Santa Barbara

10A – PUSHING THE BOUNDARIES OF MACHINE LEARNING AND SYNTHESIS

Time: 9:45 AM – 10:30 AM

Moderator: Vinicius Possani, Synopsys

This session is devoted to innovations in ML for synthesis. The first paper presents a novel technique for approximate logic synthesis using adaptive decision trees guided by explainable ML. The second paper proposes runtime-constrained reinforcement learning to generate synthesis scripts. The third paper shows that arithmetic block identification can be solved by a graph learning-based approach. The last paper introduces an application-specific circuit-based SAT solver for logic synthesis.

Sampling-Based Approximate Logic Synthesis: An Explainable Machine Learning Approach

Wei Zeng, University of Wisconsin – Madison

Azadeh Davoodi, University of Wisconsin – Madison

Rasit Onur Topaloglu, IBM

RL-Guided Runtime-Constrained Heuristic Exploration for Logic Synthesis

Yasasvi Peruvemba, Indian Institute of Technology Indore

Shubham Rai, Technische Universität Dresden

Kapil Ahuja, Indian Institute of Technology Indore

Akash Kumar, Technische Universität Dresden

Graph Learning-Based Arithmetic Block Identification

Zhuolun He, The Chinese University of Hong Kong

Ziyi Wang, The Chinese University of Hong Kong

Chen BAI, The Chinese University of Hong Kong

Haoyu Yang, NVIDIA Corp.

Bei Yu, The Chinese University of Hong Kong

A Circuit-Based SAT Solver for Logic Synthesis

He-Teng Zhang, National Taiwan University

Jie-Hong Roland Jiang, National Taiwan University

Alan Mishchenko, University of California Berkeley

10B – HARDWARE APPROACHES FOR EMBEDDED PERFORMANCE AND ROBUSTNESS

Time: 9:45 AM – 10:30 AM

Moderator: Weiwen Jiang, George Mason University

This session includes four papers that provide novel hardware-related approaches for improving embedded systems performance and robustness, including a method to accelerate sparse matrix vector multiplication by compressing the input and designing an FPGA-based hardware accelerator for efficient execution, analysis of functional and architectural features of high-bandwidth memory and their benefits for real-time systems, a lossy compressed representation of sparse matrices used in neural networks to reduce the storage and overhead and memory footprint, and a runtime register file randomization technique to improve reliability of multicores operating under staggered redundant execution.

Optimized Data Reuse via Reordering for Sparse Matrix-Vector Multiplication on FPGAs

Shiqing Li, Nanyang Technological University

Di Liu, Nanyang Technological University

Weichen Liu, Nanyang Technological University

Demystifying the Characteristics of High Bandwidth Memory for Real-Time Systems

Kazi Asifuzzaman, Barcelona Supercomputing Center

Mohamed AbuElAla, McMaster University

Mohamed Hassan, McMaster University

Francisco J Cazorla, Barcelona Supercomputing Center

dCSR: A Memory-Efficient Sparse Matrix Representation for Parallel Neural Network Inference

Elias Trommer, Infineon Technologies

Bernd Waschneck, Infineon Technologies

Akash Kumar, Technische Universität Dresden

Improving the Robustness of Redundant Execution with Register File Randomization

Ilya Tuzov, Universidad Politécnica de Valencia

Pablo Andreu, Universidad Politécnica de Valencia

Laura Medina, Universidad Politécnica de Valencia

Tomas Picornell, Universidad Politécnica de Valencia

Antonio Robles, Universidad Politécnica de Valencia

Pedro Lopez, Universidad Politécnica de Valencia

Jose Flich, Universidad Politécnica de Valencia

Carles Hernández, Universidad Politécnica de Valencia

10C – ADVANCED DESIGN VERIFICATION METHODS

Time: 9:45 AM – 10:30 AM

Moderator: Masahiro Fujita, University of Tokyo

A spectrum of advanced design verification methods is discussed. The first paper discusses software based counter-measures against attacks such as Spectre which exploit speculative execution to leak information through micro-architectural side channels. The second paper addresses verification of X-valued circuits which arise in various contexts of system design. The third paper presents a novel methodology for testing hardware model checkers using circuit mutations. The fourth paper presents a technique for mapping security properties across different levels of design abstraction facilitating design verification.

Bounded Model Checking of Speculative Non-Interference

(BPA award nominee)

Emmanuel Pescosta, TU Wien

Georg Weissenbacher, TU Wien

Florian Zuleger, TU Wien

Compatible Equivalence Checking of X-Valued Circuits

Yu-Neng Wang, National Taiwan University

Yun-Rong Luo, National Taiwan University

Po-Chun Chien, National Taiwan University

Ping-Lun Wang, National Taiwan University

Hao-Ren Wang, National Taiwan University

Wan-Hsuan Lin, National Taiwan University

Jie-Hong Roland Jiang, National Taiwan University

Chung-Yang Huang, National Taiwan University

Feedback-Guided Circuit Structure Mutation for Testing Hardware Model Checkers

Chengyu Zhang, East China Normal University

Minquan Sun, East China Normal University

Jianwen Li, East China Normal University

Ting Su, East China Normal University

Geguang Pu, East China Normal University

AutoMap: Automated Mapping of Security Properties Between Different Levels of Abstraction in Design Flow

Bulbul Ahmed, University of Florida

Fahim Rahman, University of Florida

Nick Hooten, Dynetics

Farimah Farahmandi, University of Florida

Mark Tehranipoor, University of Florida

SPECIAL SESSION 10D – SECURITY CLOSURE OF PHYSICAL LAYOUTS

Time: 9:45 AM – 10:30 AM

Moderator: Ramesh Karri, New York University

CAD tools traditionally optimize ICs for power, performance, and area. However, given a vast number of emerging security threats that are directly affecting the hardware, we argue that modern CAD tools must also adopt notions of secure hardware design, and streamline related efforts throughout the entire design flow. Indeed, the stakes are high for IC vendors and design partners, as security risks that are not assessed and mitigated throughout the design flow will become exploitable in the field, where ICs are difficult to fix, if not impossible. Prominent examples of hardware-centric threats are the retrieval of the secret AES key from a military-grade ProASIC3 chip in a fraction of a second by side-channel analysis, or the Row hammer attack that allows to leak data from access-restricted memory regions by repetitively accessing (hammering) adjacent, non-restricted regions.

This special session highlights the need and timely opportunities arising for security-focused CAD tools. Within the outlined bigger picture, this session will focus on the important notion of security closure for physical layouts -- any efforts toward secure hardware design at higher abstraction layers may become futile without such CAD support for securing the final, tape-out layouts.

This special session brings together visionary talks by government and industry leaders, and an in-depth treatment of challenges and solutions explored by researchers. With this balanced approach, the session will be useful to industry practitioners and leaders, CAD tool developers, IC designers, and hardware security researchers.

Secure back-end chip design? Why?

Shekhar Borkar, Qualcomm

Reimagining Physical Design Security

Serge Leef, DARPA

Security Closure for Physical Layouts (*Invited Paper*)

Johann Knechtel, NYU Abu Dhabi

SPECIAL SESSION 11A – HARNESSING THE POWER OF MACHINE LEARNING: EDA TO ACCELERATOR DESIGN

Time: 10:30 AM – 11:00 AM

Moderator: Krishnendu Chakrabarty, Duke University

Machine Learning (ML) has become ubiquitous in the design and optimization of circuits and systems. On one hand, ML has made profound impact on traditional VLSI CAD, in problems ranging from circuit synthesis to place-and-route. On the other hand, accelerator architectures have brought many of the complex ML algorithms to the masses. This special session will consider the interplay between ML and circuits and systems to address the following challenges: (1) How can we synthesize ML algorithms and map them to physical chip implementation? (2) How to use ML for the VLSI implementation flow? (3) How to design efficient hardware accelerators for ML algorithms? To address these key challenges, out-of-the-box approaches need to be explored. By integrating ML algorithms, data analytics, statistical modeling, and design of advanced computing systems, this session will engage a broad section of ICCAD conference attendees. This special session is targeted towards university researchers/professors, students, industry professionals, and computing system designers. This session will attract newcomers who want to learn about ML techniques for advancing hardware designs that will further empower advances in ML algorithms. Simultaneously this session will act as a catalyst for experienced researchers looking for exciting new directions in EDA methodologies, computing systems design, and multi-scale computing. This special session covers design, optimization and architecture, the three main pillars for building circuits and systems. It also highlights how ML and EDA researchers can join hands to design energy-efficient and reliable chips and systems.



Panorama Alter Peter, München Tourismus, Natalia Michalska

SPECIAL SESSION 11A – HARNESSING THE POWER OF MACHINE LEARNING: EDA TO ACCELERATOR DESIGN (CONT.)

VeriGOOD–ML: An Open–Source Flow for Automated ML Hardware Synthesis (Invited Paper)

Hadi Esmaeilzadeh, UC San Diego
Soroush Ghodrati, UC San Diego
Jie Gu, Northwestern University
Shiyu Guo, Northwestern University
Andrew B. Kahng, UC San Diego
Joon Kyung Kim, UC San Diego
Sean Kinzer, UC San Diego
Rohan Mahapatra, UC San Diego
Susmita Dey Manasi, University of Minnesota
Edwin Mascarenhas, UC San Diego
Sachin S. Sapatnekar, University of Minnesota
Ravi Varadarajan, UC San Diego
Zhiang Wang, UC San Diego
Hanyang Xu, UC San Diego
Brahmendra Reddy Yatham, UC San Diego
Ziqing Zeng, University of Minnesota

Optimizing VLSI Implementation with Reinforcement Learning (Invited Paper)

Haoxing Ren, Nvidia
Saad Godil, Nvidia
Brucek Khailany, Nvidia
Robert Kirby, Nvidia
Haiguang Liao, Nvidia
Siddhartha Nath, Nvidia
Jonathan Raiman, Nvidia
Rajarshi Roy, Nvidia

Heterogeneous Manycore Architectures Enabled by Processing-in-Memory for Deep Learning: From CNNs to GNNs (Invited Paper)

Biresh Kumar Joardar, Duke University
Aqeeb Iqbal Arka, Washington State University
Janardhan Rao Doppa, Washington State University
Partha Pratim Pande, Washington State University
Hai (Helen) Li, Duke University
Krishnendu Chakrabarty, Duke University

T1B – PARALLEL POWER GRID SOLVER AND GEOMETRY-BASED TECHNIQUES FOR ANALOG CIRCUIT DESIGN

Time: 10:30 AM – 11:00 AM

Moderator: Ibrahim Elfadel, Khalifa University

This session presents three papers on the methods of physical simulation and optimization for analog circuits. The first paper develops a highly efficient parallel iterative solver for large-scale power grid analysis based on graph spectral sparsification. The second paper addresses a common-centroid placement and routing problem. The proposed algorithms perform better in the presence of systematic variations, LDEs, layout parasitics and EM-induced degradation. The third paper uses cross-sectional images of 3-D wiring structures as input to a convolutional neural network for capacitance extraction, which shows a much faster speed than conventional tools.

pGRASS-Solver: A Parallel Iterative Solver for Scalable Power Grid Analysis Based on Graph Spectral Sparsification *(BPA award nominee)*

Zhiqiang Liu, Tsinghua University

Wenjian Yu, Tsinghua University

Performance-Aware Common-centroid Placement and Routing of Transistor Arrays in Analog Circuits

Arvind Kumar Sharma, University of Minnesota

Meghna Madhusudan, University of Minnesota

Steven Burns, Intel Corporation

Soner Yaldiz, Intel Corporation

Parijat Mukherjee, Intel Corporation

Ramesh Harjani, University of Minnesota

Sachin S. Sapatnekar, University of Minnesota

CNN-Cap: Effective Convolutional Neural Network Based Capacitance Models for Full-Chip Parasitic Extraction

Dingcheng Yang, Tsinghua University

Wenjian Yu, Tsinghua University

Yuanbo Guo, Tsinghua University

Wenjie Liang, Tsinghua University

11C – RELIABILITY: FROM INTERCONNECTS TO SYSTEMS

Time: 10:30 AM – 11:00 AM

Moderator: Puneet Gupta, University of California

This session addresses aspects of reliability at multiple levels of abstraction. The first paper builds a new scalable physics-based model for electromigration in multisegment interconnects and shows how it can be applied to analyze large interconnect systems. Next, a method for timing error detection is presented using a lightweight error-detection cell. Finally, a novel approach for low-overhead fault tolerance is presented, using principles of approximate computing to simplify logic without compromising on the accuracy of the simplified redundant system.

Analytical Modeling of Transient Electromigration Stress based on Boundary Reflections *(BPA award winner)*

Mohammad Abdullah Al Shohel, University of Minnesota

Vidya A. Chhabria, University of Minnesota

Nestor Evmorfopoulos, University of Thessaly

Sachin S. Sapatnekar, University of Minnesota

An Area-Efficient Scannable In Situ Timing Error Detection Technique Featuring Low Test Overhead for Resilient Circuits

Hao Zhang, Shanghai Jiao Tong University

Weifeng He, Shanghai Jiao Tong University

Yanan Sun, Shanghai Jiao Tong University

Mingoo Seok, Columbia University

Design Space Exploration of Approximation-Based Quadruple Modular Redundancy Circuits

Marcello Traiola, Lyon Institute of Nanotechnology

Jorge Echavarria, Friedrich-Alexander-Universität Erlangen-Nürnberg

Alberto Bosio, Lyon Institute of Nanotechnology

Jürgen Teich, Friedrich-Alexander-Universität Erlangen-Nürnberg

Ian O'Connor, Lyon Institute of Nanotechnology

SPECIAL SESSION 11D – 2021 CAD CONTEST AT ICCAD

Time: 10:30 AM – 11:00 AM

Moderator: Tsung-Wei Huang, University of Utah

The CAD Contest at ICCAD (<http://iccad-contest.org/2021/>) is a challenging, multi-month, research & development competition, focusing on advanced, real-world problems in the field of Electronic Design Automation (EDA). Contestants can participate in one or more problems provided by EDA/IC industry. The winners will be awarded at an ICCAD special session dedicated to this contest. Since 2012, the CAD Contest at ICCAD has been attracting more than a hundred teams per year, fostering productive industry-academia collaborations, and leading to hundreds of publications in top-tier conferences and journals. The contest keeps enhancing its impact and boosts EDA research.

Overview of 2021 CAD Contest at ICCAD

Tsung-Wei Huang, University of Utah

Takashi Sato, Kyoto University

Chun-Yao Wang, National Tsing Hua University

Yu-Guang Chen, National Central University

2021 ICCAD CAD Contest Problem A: Functional ECO with Behavioral Change Guidance and Benchmark Suite

Yen-Chun Fang, Cadence Design Systems, Inc.

Shao-Lun Huang, Cadence Design Systems, Inc.

Chi-An Rocky Wu, Cadence Design Systems, Inc.

Chung-Han Chou, Cadence Design Systems, Inc.

Chih-Jen Jacky Hsu, Cadence Design Systems, Inc.

Woei Tzy Wells Jong, Cadence Design Systems, Inc.

Kei-Yong Khoo, Cadence Design Systems, Inc.

2021 ICCAD CAD Contest Problem B: Routing with Cell Movement Advanced

Kai-Shun Hu, Synopsys, Inc

Tao-Chun Yu, Synopsys, Inc

Ming-Jen Yang, Synopsys, Inc

Chin-Fang Cindy Shen, Synopsys, Inc

2021 ICCAD CAD Contest Problem C: GPU Accelerated logic rewriting

Ghasem Pasandi, Nvidia

Sreedhar Pratty, Nvidia

David Brown, Nvidia

Yanqing Zhang, Nvidia

Haoxing Ren, Nvidia

Brucek Khailany, Nvidia

DATC RDF-2021: Design Flow and Beyond

Jianli Chen, IBM

Iris Hui-Ru, Jiang National
Taiwan University

Jinwook Jung, IBM

Seungwon Kim, University of
California San Diego

Andrew B. Kahng, University of
California San Diego

Victor N. Kravets, IBM

Yih-Lang Li, National Chiao Tung
University

Ravi Varadarajan, Atrienta

Mingyu Woo, University of
California San Diego

SYNOPSYS SPONSOR SESSION

Time: 11:00 AM

CAD for a More Secure Silicon Lifecycle

Mike Borza, Synopsys

THURSDAY SCHEDULE

8:00 – 12:40 PM 5 - 9:40PM CET (GERMANY), 11 PM - 3:40AM CST (CHINA)

ACCAD: 3rd Workshop on Accelerator Computer-Aided Design
(second day taking place on Friday)

7:20 – 1:30 PM 4:20 - 9:30PM CET (GERMANY), 10:20 PM - 3:30AM CST (CHINA)

AxC: 6th Workshop on Approximate Computing

9:00 – 2:40 PM 6:00 - 11:40PM CET (GERMANY), 12:00 PM - 5:40AM CST (CHINA)

HALO | Workshop on Hardware and Algorithms for Learning On-a-chip

7:20 – 1:30 PM 4:20 - 10:30PM CET (GERMANY), 10:20 PM - 4:30AM CST (CHINA)

Top Picks in Hardware and Embedded Security Workshop

7:20 – 1:30 PM 4:20 - 9:15PM CET (GERMANY), 10:20 PM - 3:15AM CST (CHINA)

Cadence Workshop – A shift-left methodology for the development of hardware accelerators in compute-intensive Edge applications

9:00 – 1:20 PM 6:20 - 10:20PM CET (GERMANY), 12 AM - 3:15AM CST (CHINA)

WOSET Workshop on Open Source EDA Technologies (Co-located Event)

6:00 – 1:25 PM 3 - 10:25PM CET (GERMANY), 9 PM - 3:25AM CST (CHINA)

SLIP: ACM/IEEE International Workshop on System-Level Interconnect Pathfinding (Co-Located Event)



Siegestor am Abend, München Tourismus, Tommy Lösch

ACCAD: WORKSHOP ON ACCELERATOR COMPUTER-AIDED DESIGN

8:00 am – 12:40 pm

Organizers:

Ibrahim (Abe) Elfadel, Khalifa University

Subhasish Mitra, Stanford University

This is the 3rd version of a trending workshop whose goal is to provide a forum to present and discuss the current trends in computer-aided design in support of domain-specific accelerator chips, especially for artificial intelligence and machine learning applications. The workshop will be concerned with the VLSI methodology flow from high-level synthesis to physical verification and performance prediction, particularly in the way it gets impacted with the emerging design paradigms of domain-specific instruction sets, approximate computing, in-memory computing, and stochastic computing. Of particular interest to the workshop are the transformations that VLSI CAD has to undergo to adapt to the post-CMOS technologies when they are considered in the context of accelerator design. The workshop will include, but will not be limited to, the following topics:

- » High-level synthesis of machine-learning accelerators
- » Design space exploration of domain-specific accelerators
- » Tools and methodologies for in-memory computing
- » Tools and methodologies for approximate computing
- » CAD for emerging accelerator technologies: ReRAM, MRAM, Photonics, etc.
- » Tools and methodologies for the post-CNN era
- » Tools and methodologies for the testing and verification of accelerator chips.

8:00 Welcome Note

Abe Elfadel and Subhasish Mitra

8:10 Keynote: Accelerating Deep Neural Networks with Analog Nonvolatile Memory Devices

Geoffrey Burr, IBM Research

9:00 Bio-Inspired AI from Edge to Cloud: SpiNNaker2 and Beyond

Christian Mayr, TU Dresden

9:40 Design Space Exploration for In-Memory Computing with Associative Memories

X. Sharon Hu, University of Notre Dame

10:30 Integrated Circuit Design Redaction through Transistor-Level Programming (TRAP)

Yiorgos Makris, UT Dallas

11:10 Hardware/Software Co-Design of Deep Learning Accelerators

Yiyu Shi, University of Notre Dame

11:50 Generation, Execution and Model Optimized Stochastic Computing Based Inference Acceleration

Puneet Gupta, UCLA

12:30 Closing Remarks of Session 1

Abe Elfadel and Subhasish Mitra

ACCAD WORKSHOP SESSION 2

8:00am – 12:00 p.m.

8.00 Welcome Note to Session 2

Abe Elfadel and Subhasish Mitra

8:10 Keynote: ReRAM-enabled and Application-Specific Co-Designed AI Accelerators

Tim Cheng, HKUST

9:00 Ensembling CNNs to Improve Robustness in Approximate Edge AI Computing

David Atienza, EPFL

9:40 OpenFPGA

Pierre-Emmanuel Gaillardon, University of Utah

10:30 The Interplay of Online and Offline Machine Learning for Industrial Design Flow Tuning

Mathew Ziegler, IBM Research

11:10 CHIMERA: Efficient DNN Training and Inference at the Edge with On-Chip Resistive RAM

Priyanka Raina, Stanford University

11:50 Closing Remarks

Abe Elfadel and Subhasish Mitra

AXC: WORKSHOP ON APPROXIMATE COMPUTING

7:20 – 12:30 am

Organizers:

Alberto Bosio, École Centrale de Lyon

Alexandra Kourfali, University of Stuttgart

Alessandro Savino, Politecnico di Torino

Jürgen Teich, Friedrich–Alexander Universität Erlangen–Nürnberg

This workshop aims at exploring the Approximate Computing (AxC) continuum, making room for the exploration of methodologies able to exploit effective and real systems that can inspire applications in many recent application domains such as machine learning, safety, and security. AxC is defined based on the intuitive observation that, while performing exact computation requires a high amount of computational resources, allowing a selective approximation or an occasional relaxation of the specification may provide significant gains in energy efficiency while still providing acceptable results. Nowadays, AxC represents a novel design paradigm for building modern systems, which offer efficiency trade-offs, between performance, power consumption, hardware area, execution timing, and the quality/exactness of the outcomes.

07:20am Opening (Welcome Message from Chairs)

07:30am Invited Talks Session

Approximate Computing for Low Power Circuits and Systems

Weiqiang Liu, Nanjing University of Aeronautics and Astronautics

Automated and Sound Approximation of Numerical Kernels

Eva Darulova, Max Planck Institute for Software Systems

Approximate Computing – The Holy Grail of Low-Energy Electronic Systems?

Jari Nurmi, Tampere University

10:00am Session1: Approximate computing in Machine Learning and DSP Applications

Neural Network Hardware Acceleration Based on Hybrid Approximate Multipliers

Si yuan Liang, Ke Chen, Pengfei Huang, Peipei Yin and Weiqiang Liu

CNN Compression through Retraining-free Weight Sharing

Etienne Dupuis, David Novo, Ian O'Connor and Alberto Bosio

Combining Logic Refactoring and Approximate Computing to Powerand Area-Efficient Gaussian Filter Designs

Marcio Monteiro, Ismael Seidel, Mateus Grellert, Jose Luis Güntzel, Leonardo Soares and Cristina Meinhardt

THURSDAY, NOVEMBER 4

11:10am Regular Session: Approximate Design Techniques

Approximate PIM: An IMPLY-based Approximate Adder
Seyed Erfan Fatemieh, Mohammad Reza Reshadinezhad and Nima Taherinejad

Assertion-aware based approximate computing
Moreno Bragaglio, Samuele Mori, Samuele Germiniani, Alberto Bosio, Marcello Traiola and Graziano Pravadelli

Task Scheduling on Mixed-Precision MPSoC
Ahmad Sadigh Baroughi, Stefan Huemer, Hadi Shahriar Shahhoseini and Nima Taherinejad

12:20pm Regular Session: Approximate Synthesis for FPGA targets

Approximation Space Exploration for FPGA Accelerators Using Fault Injection
Ioannis Tsounis, Athanasios Papadimitriou and Mihalys Psarakis

Exploring a Decision Tree Synthesis Flow for Approximate Circuits
Brunno Abreu, Jonata Carvalho, Mateus Grellert and Cristina Meinhardt

A Catalog-based AIG-Rewriting Approach to the Design of Approximate Components
Mario Barbareschi, Salvatore Barone, Nicola Mazzocca and Alberto Moriconi

1:20pm Closing Session

HALO | WORKSHOP ON HARDWARE AND ALGORITHMS FOR LEARNING ON-A-CHIP

8:20 am – 2:40 pm

Organizers: Qinru Qiu, Syracuse University;
Yingyan Lin, Rice University;
Chenchen Liu, University of Maryland

9:00am Introduction and opening remarks

9:05am Keynote

David Pan, The University of Texas at Austin

9:50am Session 1: Efficient Inference and Learning Algorithms

Session Chair:

Meng Li, Facebook
Peter Kairouz, Google
Zhiru Zhang, Cornell University

11:05pm Break

11:25pm Session 2: Algorithm-Accelerator Co-design and Compilers

Section Chair:

Jonathan Frankle, Massachusetts Institute of Technology
Yuhao Zhu, University of Rochester
Bo Yuan, Rutgers University

Session 3: Emerging Device and Neuromorphic Computing

Section Chair:

Jianhua YOSHUA Yang, University of Southern California
Xue Lin, Northeastern University
Shimeng Yu, Georgia Tech

1:55pm Keynote

Vijay Janapa Reddi, Harvard University

TOP PICKS IN HARDWARE AND EMBEDDED SECURITY WORKSHOP

7:20 – 1:30 pm

Organizers:

Gang Qu, University of Maryland, College Park

Johanna Sepulveda, Airbus Defence and Space

7:20 Welcome message from the chair (Gang Qu)

7:30 Session 1 Logic Locking

Pirates of the Carry-Boolean: Exploring Structural Artifacts of Logic Locking with SAIL

Prabuddha Chakraborty

Provably-Secure Logic Locking: From Theory to Practice

Jeyavijayan Rajendran

8:30 Session 2 Trust Execution Environment

SANCTUARY: ARMing TrustZone with User-space Enclaves

Emmanuel Stauf

HybCache: Hybrid Side-Channel-Resilient Caches for Trusted Execution Environments

Tommaso Frassetto

9:30 Session 3 Side-Channel Analysis

The Curse of Class Imbalance and Conflicting Metrics with Machine Learning for Side-channel Evaluations

Stjepan Picek

Horizontal Side-Channel Vulnerabilities of Post-Quantum Key Exchange Protocols

Aydin Aysu

10:45 Session 4 Identification: from Recycled IC to DNN

Recycled IC Detection Based on Statistical Methods

Yiorgos Makris

DeepAttest: An End-to-End Attestation Framework for Deep Neural Networks

Huili Chen

11:45 Session 5 Buffer Exploitation and Memory Safety

Secure TLBs

Shuwen Deng

SpectreRSB: Spectre attacks using the return stack buffer

Nael Abu-Ghazaleh

CHEx86: Context-Sensitive Enforcement of Memory Safety via Microcode-Enabled Capabilities

Rasool Sharifi

1:15 Closing Remarks

Johanna Sepulveda

1:00 Summary
Sarmad Dahir

WOSET: WORKSHOP ON OPEN SOURCE EDA TECHNOLOGIES (CO-LOCATED)

Please note that woset is a co-located workshop and requires a separate registration.

Please visit woset's website for more detailed information. <https://woset-workshop.github.io/>

9:00 am – 1:20 pm

Organizers:

Matthew Guthaus, UC Santa Cruz

Jose Renau, UC Santa Cruz

The WOSET co-located event aims to galvanize the open-source EDA movement. The workshop will bring together EDA researchers who are committed to open-source principles to share their experiences and coordinate efforts towards developing a reliable, fully open-source EDA flow. The workshop will feature presentations and posters that overview existing or under-development open-source tools, designs and technology libraries. A live demo session for tools in advanced state will be planned. The workshop will feature a panel on the present status and future challenges in open-source EDA, and how to coordinate efforts and ensure quality and interoperability across open-source tools. A cash award will be given for a Best Tool Award.

SHORT PAPERS

9:00

FABulous: An Open-Everything Framework For Embedded FPGAs

Bea Healy, University of Manchester

Jing Yu, University of Manchester

Nguyen Dao, University of Manchester

King Lok Chung, University of Manchester

Dirk Koch, University of Manchester

OpenCache: An Open-Source OpenRAM Based Cache Generator

Eren Dogan, Ozyegin University

Hasan Fatih Ugurdag, Ozyegin University

Matthew Guthaus, UC Santa Cruz

9:15

Towards Fast And Accurate Parallel Chip Thermal Simulations With PACT

Zihao Yuan, Boston University

Prachi Shukla, Boston University

Sofiane Chetoui, Brown university

Carlton Knox, Boston University

Sean Nemtzw, Boston University

Sherief Reda, Brown University

Ayse K. Coskun, Boston University

A Guide For Rapid Creation Of New HDLs

Sakshi Garg, University of California

Sheng-Hong Wang, University of California

Hunter James Coffman, University of California

Jose Renau, University of California

9:30

SystemVerilog IDE Integration With Verible Language Server Support

Henner Zeller, Google

RTLFuzzLab

Brandon Fajardo, UC Berkeley

Kevin Laeuffer, UC Berkeley

Jonathan Bachrach, UC Berkeley

Koushik Sen, UC Berkeley

Interact: An Interactive Design Environment For Asynchronous Logic

Jiayuan He, University of Texas at Austin

Wenmian Hua, Yale University

Yi-Shan Lu, University of Texas at Austin

Sepideh Maleki, University of Texas at Austin

Yihang Yang, Yale University

Keshav Pingali, University of Texas at Austin

Rajit Manohar, Yale University

LONG PAPERS 1

9:51

CFU Playground: Build Your Own ML Processor Using Open Source

Tim Callahan, Google

Tim Ansell, Google

Joseph Bushagour, Purdue University

Alan V. Green, Google

David Lattimore, Google

Dan Callaghan, Google

The Open-Source Bluespec Bsc Compiler And Reusable Example Designs

Julie Schwartz, Bluespec, Inc.

Niraj N. Sharma, Bluespec, Inc.

Darius Rad, Bluespec, Inc.

Ken Takusagawa, Bluespec, Inc.

Joe Stoy, Bluespec, Inc.

Rishiyur Nikhil, Bluespec, Inc.

10:21

A CMOS Programmable Analog Standard Cell Library In Skywater 130nm Open-Source Process

Jennifer Hasler, Georgia Institute of Technology

Barry Muldrey, University of Mississippi

Parker Hardy, University of Mississippi

Automating GDS Generation In Magic

Tim, Open Circuit Design

10:51

Porting Software To Hardware Using XLS/DSLX

Johan Euphrosine, Google

Rob Springer, Google

MLIR As Hardware Compiler Infrastructure

Schuyler Eldridge, SiFive

Prithayan Barua, SiFive

Aliaksei Chapyzhenka, SiFive

Adam Izraelevitz, SiFive

Jack Koenig, SiFive

Chris Lattner, SiFive

Andrew Lenharth, SiFive

George Leontiev, SiFive

Fabian Schuiki, SiFive

Ram Sunder, SiFive

Andrew Young, SiFive

Richard Xia, SiFive

POSTER PRESENTATIONS

11:30

VeZZal - a containerized tool to work with and test open source EDA tools

Sai Charan Lanka

Testing the OpenRAM Break-Out Chip Using a Raspberry Pi-Based Logic Analyzer

Aiden Dullaghan

Developing Open-Source Circuit Design and Flow Management Software

Maxwell Chen, Poolesville High School

R. Timothy Edwards, Efabless

Software Inspired IC Hardware Workflows Using Bazel

Ethan Mahintorabi, Google

LONG PAPERS 2

11:50

A Toolkit For Designing Hardware DSLs

Griffin Berlstein, Cornell University
Rachit Nigam, Cornell University
Chris Gyurgyik, Cornell University
Adrian Sampson, Cornell University

LSOracle 2.0: Capabilities, Integration, And Performance

Scott Temple, University of Utah
Ashton Snelgrove, University of Utah
Walter Lau Neto, University of Utah
Pierre-Emmanuel Gaillardon, University of Utah

12:20

Open-Source Formal Verification For Chisel

Kevin Laeuffer, University of California, Berkeley
Jonathan Bachrach, University of California, Berkeley
Koushik Sen, University of California, Berkeley

Towards Functional Coverage-Driven Fuzzing For Chisel Designs

Andrew Dobis, Technical University of Denmark
Tjark Petersen, Technical University of Denmark
Martin Schoeberl, Technical University of Denmark

12:50

A Parallel HDL Compilation Framework

Sheng-Hong Wang, University of California
Sakshi Garg, University of California
Hunter James Coffman, University of California
Kenneth Mayer, University of California
Jose Renau, University of California

ESSENT: A High-Performance RTL Simulator

Sakshi Garg, University of California
Sheng-Hong Wang, University of California
Hunter James Coffman, University of California
Jose Renau, University of California

SLIP: ACM/IEEE INTERNATIONAL WORKSHOP ON SYSTEM-LEVEL INTERCONNECT PATHFINDING (CO-LOCATED)

Please note that SLIP is a co-located workshop and requires a separate registration.

Please visit SLIP's website for more detailed information <http://www.sliponline.org/>

6:00 am – 1:25 pm

Organizer:

Mustafa Badaroglu, Qualcomm; **Brian Cline**, Arm; **Ismail Bustany**, Xilinx

The 23rd ACM/IEEE International Workshop on System-Level Interconnect Pathfinding (SLIP 2021), co-hosted with ICCAD 2021, will bring together researchers and practitioners who have a shared interest in the challenges and futures of system-level interconnect, coming from wide-ranging backgrounds that span system, application, design, and technology.

6:00 General Chair Message – Welcome Message & Opening Remarks

Mustafa Badaroglu, Qualcomm

6:15 Session 1 – System Technology Co-Optimization for Advanced Physical Design

Session Chair: Yuzo Fukuzaki, TechInsights & **Ivan Ciofi**, imec

A novel system-level physics-based electromigration modelling framework; Application to the power delivery network

Houman Zahedmanesh, **Ivan Ciofi**, **Odysseas Zografos**, **Mustafa Badaroglu**, and **Kristof Croes**

Design and system technology co-optimization sensitivity prediction for VLSI technology development using machine learning

Chung-Kuan Cheng, **Chia-Tung Ho**, **Chester Holtz**, and **Bill Lin**

Enabling chiplet integration beyond 7nm (Invited Talk)

Suresh Ramalingam

7:40 Session 2 – 3D EDA and Security

Session Chair: Shantanu Dutt, University of Illinois at Chicago & **Seungwon Kim**, University of California

Design and sign-off methodologies for wafer-to-wafer bonded 3D-ICs at advanced nodes (Invited)

Giuliano Sisto, **Rongmei Chen**, **Richard Chou**, **Geert Van der Plas**, **Eric Beyne**, **Rod Metcalfe** and **Dragomir Milojevic**

Chip stacking and packaging technology explorations for hardware security (Invited Talk)

Makoto Nagata

Performance-aware interconnect delay insertion against EM side-channel attack

Minmin Jiang and **Vasilis Pavlidis**

9:05 Keynote Address — Recent advances and future challenges in 2.5D/3D heterogeneous integration

Session Chair: Brian Cline, ARM

Tanay Karnik, Intel Corp. **Session Chair: Ismail Bustany**, Xilinx

9:55 Session 3 — Next Generation Optical Interconnects

Session Chair: Dirk Stroobandt, Ghent University; **Rasit Topaloglu**, IBM
Reconfigurable on-chip wireless interconnections through optical phased arrays

Giovanna Calò, Gaetano Bellanca, Davide Bertozzi, Marina Barbiroli, Franco Fuschini, Giovanni Serafino, Velio Tralli, and Vincenzo Petruzzelli

Silicon photonics technology for terabit-scale optical I/O (Invited Talk)

Joris Van Campenhout

Designing a multi-chiplet manycore system using the POPSTAR optical NoC architecture (Invited Talk)

Yvain Thonnart

11:20 Session 4 — 3D Interconnects and Networks-on-Chips

Session Chair: Pascal Vivet, CEA & **Poona Bahrebar**, Ghent University

The open domain-specific architecture: An introduction (Invited Talk)

Bapi Vinnakota

SID-Mesh: Diagonal mesh topology for silicon interposer in 2.5D NoC with introducing a new routing algorithm

Babak Sharifpour, Mohammad Sharifpour, and Midia Reshadi

RAMAN: Reinforcement learning inspired algorithm for mapping applications onto mesh Network-on-Chip

Jitesh Choudhary, Soumya J, and Linga Reddy Cenkeramaddi

Network-on-Chips for future 3D stacked dies (Invited Talk)

Tiago Mück

1:15pm General Chair Closing Remarks — Audience Poll & Closing Remarks

Mustafa Badaroglu, Qualcomm

FRIDAY SCHEDULE (IN-PERSON EVENT)

10:00 – 11:00 AM CET

Keynote: Designing Reliable Distributed Systems
Dirk Ziegenbein, Robert Bosch GmbH

11:30 AM – 12:30PM CET

Technical Papers Session: Security and System-Level CAD

12:30 PM – 1:30PM CET

Lunch

1:30 – 2:30PM CET

Technical Papers Session: Back to the Future: EDA for Emerging Technologies

2:30 – 3:30 PM CET

Poster Session & Networking Break

3:30 – 4:30PM CET

Panel: Security meets Open-Source Hardware and Tools: Friend or Foe?

4:30 – 5:30PM CET


Panel: Future of Academia-Industry Engagement in EDA for Research and Education

5:30 – 6:30PM CET

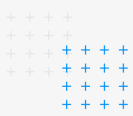
Closing & Bus Transfer to Resturant

6:30 – 10:00PM CET

Social Dinner & Networking



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SESSION 12 | SECURITY AND SYSTEM-LEVEL CAD

Time: 11:30 PM – 12:30 PM

Moderator: Daniel Tille, Infineon Technologies AG

BigIntegr: One-Pass Architectural Synthesis for Continuous-Flow Microfluidic Lab-on-a-Chip Systems

Xing Huang, Technical University of Munich

Youlin Pan, Fuzhou University

Zhen Chen, Fuzhou University

Wenzhong Guo, Fuzhou University

Robert Wille, Johannes Kepler University Linz

Tsung-Yi Ho, National Tsing Hua University

Ulf Schlichtmann, Technical University of Munich

dCSR: A Memory-Efficient Sparse Matrix Representation for Parallel Neural Network Inference

Elias Trommer, Infineon Technologies

Bernd Waschneck, Infineon Technologies

Akash Kumar, Technische Universität Dresden

Engineering an Efficient Boolean Functional Synthesis Engine

(BPA award nominee)

Priyanka Golia, Indian Institute of Technology Kanpur, National University of Singapore

Friedrich Slivovsky, TU Wien

Subhajit Roy, Indian Institute of Technology Kanpur

Kuldeep S. Meel, National University of Singapore

RL-Guided Runtime-Constrained Heuristic Exploration For Logic Synthesis

Yasasvi Peruvemba, Indian Institute of Technology Indore

Shubham Rai, Technische Universität Dresden

Kapil Ahuja, Indian Institute of Technology Indore

Akash Kumar, Technische Universität Dresden

LoopBreaker: Disabling Interconnects to Mitigate Voltage-Based Attacks in Multi-Tenant FPGAs

Hassan Nassar, Karlsruher Institut für Technologie

Hanna Al Zughbi, Independent

Dennis Gnad, Karlsruher Institut für Technologie

Lars Bauer, Karlsruher Institut für Technologie

Mehdi Tahoori, Karlsruher Institut für Technologie

Jörg Henkel, Karlsruher Institut für Technologie

Aker: A Design and Verification Framework for Safe and Secure SoC Access Control

Francesco Restuccia, Scuola Superiore Sant'Anna Pisa

Andres Meza, University of California, San Diego

Ryan Kastner, University of California, San Diego

SESSION 13 | BACK TO THE FUTURE: EDA FOR EMERGING TECHNOLOGIES

Time: 1:30 PM – 2:30 PM

Moderator: Stephan Eggersgluß, Siemens Digital Industries Software

Exploring Physical Synthesis for Circuits based on Emerging Reconfigurable Nanotechnologies

Andreas Krinke, Technische Universität Dresden

Shubham Rai, Technische Universität Dresden

Akash Kumar, Technische Universität Dresden

Jens Lienig, Technische Universität Dresden

Peripheral Circuitry Assisted Mapping Framework for Resistive Logic-In-Memory Computing

Shuhang Zhang, Technical University of Munich

Hai (Helen) Li, Duke University

Ulf Schlichtmann, Technical University of Munich

Optimal Mapping for Near-Term Quantum Architectures based on Rydberg Atoms

Sebastian Brandhofer, University of Stuttgart

Hans Peter Büchler, University of Stuttgart

Ilia Polian, University of Stuttgart

ToPro: A Topology Projector and Waveguide Router for Wavelength-Routed Optical Networks-on-Chip

Zhidan Zheng, Technical University of Munich

Mengchu Li, Technical University of Munich

Tsun-Ming Tseng, Technical University of Munich

Ulf Schlichtmann, Technical University of Munich

Manufacturing Cycle-Time Optimization Using Gaussian Drying Model for Inkjet-Printed Electronics

Tsun-Ming Tseng, Technical University of Munich

Meng Lian, Technical University of Munich

Mengchu Li, Technical University of Munich

Philipp Rinklin, Technical University of Munich

Leroy Grob, Technical University of Munich

Bernhard Wolfrum, Technical University of Munich

Ulf Schlichtmann, Technical University of Munich

POSTER SESSION & NETWORKING BREAK

Time: 3:30 – 4:30 PM

PANEL: SECURITY MEETS OPEN-SOURCE HARDWARE AND TOOLS: FRIEND OR FOE?

Time: 4:30 – 5:30 PM

Organizer: Georg Sigl, Technical University of Munich

With the rise of RISC-V, open-source hardware has become reality. Not just the architecture but also designs are developed open source. This means that at least RTL-code is publicly available. With open-source tools and libraries, even lower levels of design data will become public. This can, on the one hand, jeopardize hiding attempts for cryptographic keys or put ideal attack locations on the spot, thus compromising security. On the other hand, development of open-source hardware trust anchors increase the availability of such IP cores and allows integration in system-on-chips (SoC), thus improving security of future products. There they can be used, e.g., to ensure secure boot processes, protect software updates, and cryptographic authentication of these SoCs. Open source allows security verification for everybody and therefore improves transparency and trust in such hardware trust anchors. At the same time, it has a significant impact on the business for semiconductor vendors offering such trust anchors as dedicated chips.

The panel aims to discuss the impact of open-source hardware on the business, technical sovereignty, security and tries to identify the trends for the next years. The panelists cover the complete industrial value chain of trusted electronics and research in the area of secure hardware as well as tools.

Moderator:

Georg Sigl, Technical University of Munich

Panelists:

Detlef Houdeau, Infineon Technologies AG

Sascha Kegreiss, HENSOLDT Cyber

Johanna Sepulveda, Airbus Defence and Space

Iliia Polian, University of Stuttgart

Johann Heyszl, Fraunhofer AISEC

FUTURE OF ACADEMIA-INDUSTRY ENGAGEMENT IN EDA FOR RESEARCH AND EDUCATION

Time: 4:30 – 5:30 PM

Moderator:

Ulf Schlichtmann, Technical University of Munich

Panelists:

Anton Klotz, Cadence Design Systems

Patrick Haspel, Synopsys

Frank Schenkel, MunEDA

Raik Brinkmann, Siemens AG

CLOSING & BUS TRANSFER TO RESTAURANT

Time: 5:30 – 6:30 PM

SOCIAL DINNER & NETWORKING

Time: 6:30 – 10:00 PM

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1) SYSTEM-LEVEL CAD

1.1 System Design

- » System-level specification, modeling, simulation, design flows
- » System-level issues for 3D integration
- » System-level design case studies and applications
- » HW/SW co-design, co-simulation, co-optimization, and co-exploration, platforms for emulation and rapid prototyping
- » Micro-architectural transformation
- » Multi-/many-core processor, GPU and heterogeneous SoC
- » Memory and storage architecture and system synthesis
- » System communication architecture, Network-on-chip design
- » Modeling, simulation, high-level synthesis, power/performance analysis, programming of heterogeneous computing platforms
- » Application driven system design for big data
- » Analysis and optimization of data centers

1.2 Embedded, Cyber-Physical (CPS), IoT Systems and Software

- » AI and machine learning for embedded systems
- » HW/SW co-design for embedded systems
- » Compute, memory, storage, interconnect for embedded systems
- » Domain-specific accelerators
- » Energy/power management and energy harvesting
- » Real-time software and systems
- » Middleware, virtual machines, and runtime support
- » Dependable, safe, secure, trustworthy embedded systems
- » Embedded software: compilation, optimization, testing
- » CAD for IoT, edge and fog computing
- » Modeling, analysis, verification of CPS systems
- » Green computing (smart grid, energy, solar panels, etc.)
- » CAD for application domains including wearables, health care, autonomous systems, smart cities

1.3 Neural Networks and Deep Learning

- » Hardware and architecture for neural networks
- » Compilers for deep neural networks
- » Design method for learning on a chip
- » System-level design for (deep) neural computing
- » Neural network acceleration including GPU and ASICs
- » Safe and secure machine learning
- » Hardware accelerators for Artificial Intelligence

1.4 Reconfigurable Computing

- » Novel reconfigurable architectures (FPGA, CGRA, etc.)
- » Neural network acceleration on reconfigurable accelerators
- » High-level synthesis on reconfigurable architectures
- » Compilers for reconfigurable architectures
- » Reconfigurable fabric security
- » HW/SW prototyping and emulation on FPGAs
- » Post-synthesis optimization for FPGAs
- » FPGA-based prototyping for analog, mixed-signal, RF systems

1.5 Hardware Security, Security Architecture and Systems

- » Hardware Trojans, side-channel attacks, fault attacks and countermeasures
- » New physical attack vectors or methods for ASICs
- » Nano electronic security
- » Hardware-based security (CAD for PUF's, RNG, AES etc.)
- » Split Manufacturing for security
- » Supply chain security and anti-counterfeiting
- » Artificial Intelligence for attack prevention systems
- » Design and CAD for security
- » Security implications of CAD
- » Trusted execution environments
- » Privacy-preserving computation
- » Cloud Computing data security
- » Sensor network security

1.6 Low Power and Approximate Computing in System Design

- » Power and thermal estimation, analysis, optimization, and management techniques for hardware and software systems
- » Energy- and thermal-aware application mapping and scheduling
- » Energy- and thermal-aware architectures, algorithms
- » Energy- and thermal-aware dark silicon system design
- » Hardware techniques for approximate/stochastic computing

2) SYNTHESIS, VERIFICATION, PHYSICAL DESIGN, ANALYSIS, SIMULATION, AND MODELING

2.1 High-Level, Behavioral, and Logic Synthesis and Optimization

- » High-level/Behavioral/Logic synthesis
- » Technology-independent optimization and technology mapping
- » Functional and logic timing ECO (engineering change order)
- » Resource scheduling, allocation, and synthesis
- » Interaction between logic synthesis and physical design

2.2 Testing, Validation, Simulation, and Verification

- » High-level/Behavioral/Logic modeling, validation, simulation
- » Formal, semi-formal, and assertion-based verification
- » Equivalence and property checking
- » Emulation and hardware simulation/acceleration
- » Post-silicon validation and debug
- » Digital fault modeling and simulation
- » Delay, current-based, low-power test
- » ATPG, BIST, DFT, and compression
- » Memory test and repair
- » Core, board, system, and 3D IC test

2.3 Cell-Library Design, Partitioning, Floorplanning, Placement

- » Cell-library design and optimization
- » Transistor and gate sizing
- » High-level physical design and synthesis
- » Estimation and hierarchy management
- » 2D and 3D partitioning, floorplanning, and placement
- » Post-placement optimization
- » Buffer insertion and interconnect planning

2.4 Clock Network Synthesis, Routing, and Post-Layout Optimization and Verification

- » 2D and 3D clock network synthesis
- » 2D and 3D global and detailed routing
- » Package-/Board-level
- » Chip-package-board co-design
- » Post-layout/-silicon optimization
- » Layout and routing issues for optical interconnects

2.5 Design for Manufacturability and Design for Reliability

- » Process technology characterization, extraction, and modeling
- » CAD for design/manufacturing interfaces
- » CAD for reticle enhancement and lithography-related design
- » Variability analysis and statistical design and optimization
- » Yield estimation and design for yield
- » Physical verification and design rule checking
- » Machine learning for smart manufacturing and process control
- » Analysis and optimization for device-level reliability issues
- » Analysis optimization for interconnect reliability issues
- » Reliability issues related to soft errors
- » Design for resilience and robustness

2.6 Timing, Power and Signal Integrity Analysis and Optimization

- » Deterministic and statistical static timing analysis, optimization
- » Power and leakage analysis and optimization
- » Circuit and interconnect-level low power design issues
- » Power/ground network analysis and synthesis
- » Signal integrity analysis and optimization

2.7 CAD for Analog/Mixed-Signal/RF and Multi-Domain Modeling

- » Analog, mixed-signal, and RF noise modeling, simulation, test
- » Electromagnetic simulation and optimization
- » Device, interconnect and circuit extraction and simulation
- » Behavior modeling of devices and interconnect
- » Package modeling and analysis
- » Modeling of complex dynamical systems (molecular dynamics, fluid dynamics, computational finance, etc.)

3) CAD FOR EMERGING TECHNOLOGIES, PARADIGMS

3.1 Bio-inspired and Neuromorphic Computing, Biological Systems and Electronics, and New Computing Paradigms

- » Network and neuron models
- » Devices and hardware for neuromorphic computing
- » Non-von Neumann architectures
- » PEvent or spike-based hardware systems
- » CAD for biological computing systems
- » CAD for synthetic biology
- » CAD for bio-electronic devices, bio-sensors, MEMS Systems

3.2 Nanoscale and Post-CMOS Systems

- » New device structures and process technologies
- » New memory technologies (flash, PCM, STT-RAM, memristor)
- » Nanotechnologies, nanowires, nanotubes, graphene, etc.
- » Quantum computing
- » CAD for mixed-domain (semiconductor, nanoelectronic, MEMS, and electro-optical) devices, circuits, and systems
- » CAD for nanophotonics and optical devices/ communication
- » DFM and reliability issues for emerging devices (3D, Nano photonics, non-volatile logic/memory, etc.)
- » Device, interconnect and circuit extraction and simulation
- » Behavior modeling of devices and interconnect
- » Package modeling and analysis
- » Modeling of complex dynamical systems (molecular dynamics, fluid dynamics, computational finance, etc.)

SUBMISSION DETAILS

Paper submissions must be made through the online submission system at the ICCAD web site.

Regular papers will be reviewed as finished papers; preliminary submissions will be at a disadvantage. Research papers with open-source software are highly encouraged where the software will be made publicly available (via GitHub or similar) with the camera-ready version if the paper has been accepted. For protecting the authors' identities in the double-blind review process, please do not include direct link to the non-anonymized software yet in the submitted paper but indicate the open-source contribution on a textual basis only. Authors wanting to share GitHub repositories may want to look into using <https://anonymous.4open.science/> which is an open-source tool that helps you to quickly Double-blind your repository.

Authors are asked to submit their work in two stages. In stage one (abstract submission), a title, abstract, and a list of all co-authors must be submitted via the ICCAD web submission site. In stage two (paper submission), the paper itself is submitted whereby the submitted abstract of stage one can still be modified. Authors are responsible for ensuring that their paper submission meets all guidelines, and that the PDF is readable.

DEADLINE FOR ABSTRACT AND PAPER SUBMISSIONS

The submission deadline for paper is in May of 2022.

We always have several authors contact the ICCAD office asking for a deadline extension. Due to the limited review cycle, NO extensions will be granted for ANY reason.

REGULAR PAPER SUBMISSIONS

- » All papers must be in PDF format only, with savable text and embedded fonts in included (vector) graphics.
- » Each paper must be no more than 8 pages (including the abstract, figures and tables), double-columned, 9pt or 10pt font. One page of references is allowed, which does not count towards this 8-page limitation.
- » Your submission must not include information that serves to identify the authors of the manuscript, such as name(s) or affiliation(s) of the author(s), anywhere in the manuscript, abstract, or in the embedded PDF data. References and bibliographic citations to the author(s) own published works or affiliations should be made in the third person.
- » Submissions not adhering to these rules, or determined to be previously published or simultaneously submitted to another conference, or journal, will be summarily rejected. Internal memoranda with full content not publicly available, and with author names not divulged, may be submitted.

IMPORTANT: Final camera-ready versions must be identical to the submitted papers with the following exceptions; inclusion of author names/affiliation, correction of identified errors, addressing reviewer demanded changes. No other modifications of any kind are allowed including modification of title, change of the author list, reformatting, restyling, rephrasing, removing figures/results/text, etc. The TPC Chairs reserve the right to finally reject any manuscripts not adhering to these rules.

TEMPLATES

Paper templates are available at the ICCAD website and authors are recommended to format their papers based on the ACM template.

NOTIFICATION OF ACCEPTANCE

Authors will be notified of acceptance in July of 2022. Final paper guidelines will be sent at that time.

PROCEEDINGS

The deadline for final papers is in August of 2022. Accepted regular papers are allowed six pages plus one page of references in the conference proceedings free of charge. Each additional page (except references) beyond six pages is subject to the page charge at \$150.00 per page up to the eight-page plus one page of references. ACM will hold the copyright for ICCAD 2021 proceedings. Authors of accepted papers must sign an ACM copyright release form for their paper.

CONFERENCE REGISTRATION

At least one author per accepted regular paper or poster must register in the conference, at the discounted speaker's registration rate. Failure to register will result in your paper being removed from the conference proceedings. In case of a regular paper, ACM reserves the right to exclude a paper from distribution after the conference (e.g., removal from ACM Digital Library) if the paper is not presented at the conference.

ACM/IEEE WILLIAM J. MCCALLA ICCAD BEST PAPER AWARD

The awards are split into three categories. Two papers from this year's ICCAD conference, one from front-end and one from back-end, will receive this prestigious award. The winners will be chosen from nominated papers after a thorough and competitive process by area-specific selection committees and announced at the opening session.

ICCAD TEN-YEAR RETROSPECTIVE MOST INFLUENTIAL PAPER AWARD

One paper from the 2012 and 2013 editions of ICCAD will be selected for the 10-year retrospective most influential paper award as evidenced by impact on the research community reflected in citations, on the vendor community via its use in an industrial setting, or by initiating new research venues during the past decade. Nominations from the community are welcome and can be sent to Jinjun Xiong, Technical Program Vice Chair at jinjun@buffalo.edu.

CALL FOR PROPOSALS

Call for Workshop, Tutorial, Special Session, Panel and Keynote Proposals are all due in May of 2022.

WORKSHOP PROPOSALS

ICCAD provides a vibrant and supportive environment for small-to-medium-sized affiliated workshops. Typical workshops are one-day events on the Thursday of ICCAD. All workshop proposals should be submitted through the ICCAD website or sent to the Workshop Chair.

TUTORIAL PROPOSALS

All ICCAD tutorials are embedded in the main technical program and free to conference attendees, providing value to attendees and a good audience for presenters. Typical tutorials run 1.5-2 hours, although longer tutorials (consisting of two session blocks of 1.5-2 hours each) may be considered. Tutorial suggestions should not exceed two pages, should describe the topic and intended audience, and must include a list of suggested participants with biographical data. Proposals should focus on the state-of-the-art in a specific area of broad interest amongst ICCAD attendees. All tutorial proposals should be submitted through the ICCAD website or sent to Robert Wille, Tutorial and Special Sessions Chair, at robert.wille@jku.at.

SPECIAL SESSION PROPOSALS

Special Sessions typically run 1.5-2 hours. Special session proposals should focus on in-depth treatment on a topic of timely interest to the ICCAD audience. Special session proposals should not exceed two pages, should describe the topic and intended audience, and must include a list of suggested participants with biographical data. All special session proposals should be submitted through the ICCAD website or sent to Robert Wille, Tutorial and Special Sessions Chair, at robert.wille@jku.at.

PANEL PROPOSALS

Panel suggestions should not exceed two pages, should describe the topic and intended audience, and should include a list of suggested participants. Panel suggestions must include a bulleted outline of covered topics. All panel proposals should be sent to Evangeline Young, Program Chair at fyyoung@cse.cuhk.edu.hk.

KEYNOTE PROPOSALS

Keynote proposals should include descriptions of suggested keynote speakers, and the importance of the speech to the ICCAD audience. All keynote proposals should be sent to Tulika Mitra, General Chair, at tulika@comp.nus.edu.sg. ICCAD reserves the right to restructure all panel, special session, and tutorial proposals.

IF YOU NEED ASSISTANCE, PLEASE CONTACT THE APPROPRIATE COMMITTEE MEMBERS

General Chair: Tulika Mitra, tulika@comp.nus.edu.sg

Program Chair: Evangeline Young, fyyoung@cse.cuhk.edu.hk