IEEE/ACM ICCAD
2011 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN

FINAL PROGRAM

NOVEMBER 7 - 10, 2011
SAN JOSE, CA

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IEEE/ACM ICCAD 2011 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN

ICCAD continues to be the premier conference devoted to technical innovations in design automation.

ICCAD's program of technical papers, tutorials, panels, and keynote highlight the most important current and future research challenges. A day of workshops on hot topics caps a week of non-stop technical excitement. And as always, a large number of side meetings and social events provide plenty of opportunities for networking and meeting colleagues and friends.

This year's ICCAD starts on Monday, November 7 and continues through Wednesday, November 9. You will find up-to-date details on the conference website, http://www.iccad.com.

The core of ICCAD has always been the contributed research paper program. We received 349 worldwide submissions and the technical program committee, after careful deliberation, selected 106 excellent papers for presentation. These papers are split into 26 sessions over the three days of the technical program.

In parallel with the technical program of submitted papers, ICCAD 2011 features a full track of invited, tutorial, and special sessions. These sessions, given by world experts, are an excellent opportunity for updating your knowledge in state-of-the-art and emerging areas. Two "Designer Perspective" sessions highlight contemporary needs and gaps in EDA tools. This year we resume the traditional ICCAD panel series, exploring future EDA trends on Monday evening, and continuing discussion of the impact of parallel computation on Wednesday afternoon.

ICCAD continues to host one-day topical workshops providing focused coverage of topics of emerging and current interest. This year, four workshops, on lithography, variability modeling/characterization, constraints in formal verification and adaptive power management will take place on Thursday, November 10. This year's CANDE workshop will also be co-located with ICCAD in San Jose, and held in parallel with ICCAD workshops on Thursday, November 10.

Finally, ICCAD 2011 is privileged to have a keynote address from Dr. Georg Sigl of Technische Univ. München. Prof. Sigl will provide unique insights into the design of secure hardware systems, and asks what role EDA will play in the design of future secure systems.

I hope you enjoy a week of ICCAD activities!

Joel Phillips
General Chair
Cadence Research Labs

IEEE/ACM ICCAD 2011 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN

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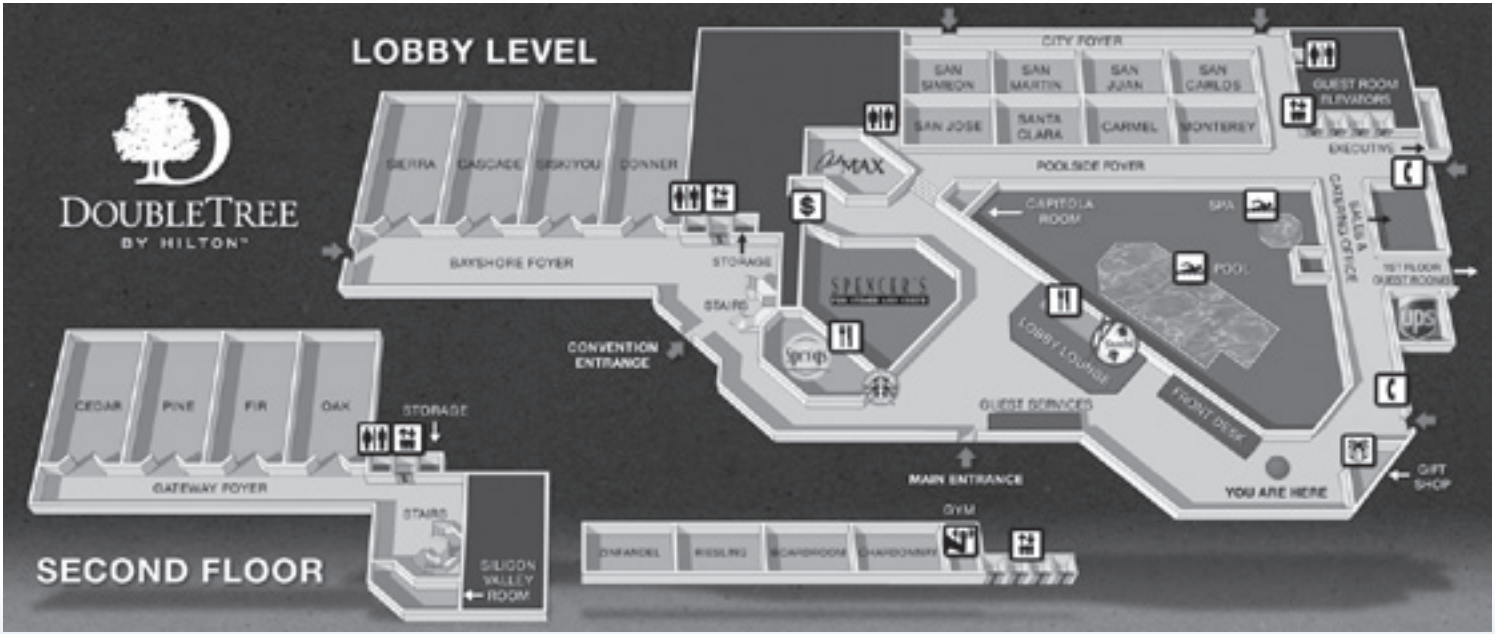

Best Paper Candidates/Award Committee

Best Paper Award Committee

Helmut Graeb
Technische Univ. München

Azadeh Davoodi
Univ. of Wisconsin

Martin D. F. Wong
Univ. of Illinois

Yao-Wen Chang
National Taiwan Univ.

Alper Demir
Koc Univ.

Luis Miguel Silveira
INSEC-ID

Sachin Sapatnekar
Univ. of Minnesota

IEEE/ACM William J. McCalla ICCAD Best Paper Award Candidates

Monday Sessions

1A.1 LAYOUT DECOMPOSITION FOR TRIPLE PATTERNING LITHOGRAPHY
Bei Yu, Boyang Zhang, Duo Ding, David Z. Pan - *Univ. of Texas, Austin*
Kun Yuan - *Cadence Design Systems, Inc.*

2A.1 A SIMPLR METHOD FOR ROUTABILITY-DRIVEN PLACEMENT
Jin Hu, Myung-Chul Kim, Dong-Jin Lee, Igor L. Markov - *Univ. of Michigan*

2B.2 OPTIMAL STATISTICAL CHIP DISPOSITION
Vladimir Zolotov, Jinjun Xiong - *IBM T.J. Watson Research Ctr.*

2C.1 IMPROVING SHARED CACHE BEHAVIOR OF MULTITHREADED OBJECT-ORIENTED APPLICATIONS IN MULTICORES
Mahmut Kandemir, Shekhar Srikantaiah - *Pennsylvania State Univ.*
Seung Woo Son - *Argonne National Lab*

TuesdaySessions

4A.1 MGR: MULTI-LEVEL GLOBAL ROUTER
Yue Xu,Chris Chu - *Iowa State Univ. and Cadence Design Systems, Inc.*
Chris Chu - *Iowa State Univ.*

7B.1 MODEL ORDER REDUCTION OF FULLY PARAMETERIZED SYSTEMS BY RECURSIVE LEAST SQUARE OPTIMIZATION
Zheng Zhang, Luca Daniel - *Massachusetts Institute of Technology*
Ibrahim (Abe) M. Elfadel - *Masdar Institute of Science and Tech.*

Wednesday Sessions

9B.1 FORMAL VERIFICATION OF PHASE-LOCKED LOOPS USING REACHABILITY ANALYSIS AND CONTINUIZATION
Matthias Althoff, Akshay Rajhans, Bruce Krogh, Soner Yaldiz, Xin Li, Larry Pileggi - *Carnegie Mellon Univ.*

9C.1 CACTI-P: ARCHITECTURE-LEVEL MODELING FOR SRAM-BASED STRUCTURES WITH ADVANCED LEAKAGE REDUCTION TECHNIQUES
Sheng Li, Norm Jouppi - *Hewlett-Packard Labs.*
Ke Chen - *Univ. of Notre Dame and Hewlett-Packard Labs.*
Jay Brockman - *Univ. of Notre Dame*
Jung Ho Ahn - *Seoul National Univ.*

10A.1 GATE SIZING AND DEVICE TECHNOLOGY SELECTION ALGORITHMS FOR HIGH-PERFORMANCE INDUSTRIAL DESIGNS
Muhammet Mustafa Ozda, Steven Burns - *Intel Corp.*
Jiang Hu - *Texas A&M Univ.*

IEEE/ACM ICCAD 2011 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN

The CADathlon at ICCAD

ACM/SIGDA sponsors the ninth annual EDA programming contest at ICCAD

Sunday, November 6, 8:00am - 5:00pm Donner Ballroom

In the spirit of the long-running ACM programming contest, the CADathlon challenges students in their CAD knowledge, and their problem solving, programming, and teamwork skills. It serves as an innovative initiative to assist in the development of top students in the EDA field. The contest will provide a platform for SIGDA, academia, and industry to focus attention on the best and brightest of next generation CAD professionals.

The students will be given a number of problems that range in difficulty and topics. Information about the CAD areas, relevant papers, and potentially a software framework that will run on Linux will be released one week before the competition. Students will be allowed to work in teams of two. At the contest, students will be given the problem statements and an example test data, but they will not have the judges' test data. Solutions will be judged on correctness and efficiency. The team that passes the most testcases is declared the winner. A handsome prize awaits the winning team. The judges are experts in EDA from both academia and industry.

During the competition students will be presented with six problems in the following areas:

- Circuit Design & Analysis
- Physical Design
- Logic & High-Level Synthesis
- System Design & Analysis
- Functional Verification
- Bio-EDA

The competition is open to all graduate students specializing in CAD currently enrolled full-time in a Ph.D. granting institution in any country. Partial or full travel grants will be provided for qualifying students.

CADathlon Organizing Committee:

Chair: Jarrod Roy
Vice Chair: Srinivas Katkoori
Vice Chair: Sudeep Pasricha
Vice Chair: Sudarshan Banerjee

http://www.sigda.org/programs/cadathlon

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Si2 (Silicon Integration Initiative) is the largest organization of industry-leading semiconductor, systems, EDA and manufacturing companies focused on the development and adoption of standards to improve the way integrated circuits are designed and manufactured, in order to speed time-to-market, reduce costs, and meet the challenges of sub-micron design. Now in its 23rd year, Si2 is uniquely positioned to enable timely collaboration through dedicated staff and a strong implementation focus driven by its member companies. Si2 represents nearly 100 companies throughout the world.

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Monday, November 7, 2011

	Registration	*7:00am - 6:00pm*	*Gateway Foyer*
	Speaker's Breakfast	*7:30 - 8:30am*	*Donner/Siskiyou Ballroom*
	AV Practice Rooms	*7:00am - 6:00pm*	*Chardonnay, Riesling, Zinfandel*
9:00 AM — TO — 10:30 AM	***Opening Session & Award Presentation***		
	Keynote Address: *Design of Secure Systems - Where are the EDA Tools? - Georg Sigl, Technische Univ. München*		***Oak/Fir Ballroom***

Coffee Break - Gateway Foyer

	Oak Ballroom	Fir Ballroom	Pine Ballroom	Cedar Ballroom
11:00 AM — TO — 12:30 PM	***Tutorial 1*** *GPU Programming for EDA with OpenCL*	***Session 1A*** *Beyond Printing Single*	***Session 1B*** *Memory and Delay Test*	***Session 1C*** *Manufacturing-Aware Optimizing Power, Performance and Reliability of the Memory Hierarchy of Embedded Systems*
	Lunch - Donner/Siskiyou Ballroom			
2:00 PM — TO — 4:00 PM	***Special Session 1*** *The ABCs of Formal Verification: Models, Algorithms, and Methodologies in RTL- and ESL-based Design Flows*	***Session 2A*** *Placement and Clocking*	***Session 2B*** *Recent Advances in Behavioral Modeling and Timing Analysis*	***Session 2C*** *Caches and Parallel Embedded Software*
	Coffee Break - Gateway Foyer			
4:30 PM — TO — 6:00 PM	***Special Session 2*** *The Role of EDA in Digital Print Automation and Infrastructure Optimization*	***Session 3A*** *DFM: From Test Structures to Computation*	***Session 3B*** *High-level and Sequential Synthesis*	***Session 3C*** *Addressing the Physical Challenges of NoC Design*

Reception - Gateway Foyer

6:30 - 7:30pm - PANEL: 2020 Vision: *What the Recent History of EDA will Look Like in Nine Years* ***- Oak/Fir Ballroom***

7:30 - 9:00pm - ACM/SIGDA Member Meeting - Donner/Siskiyou Ballroom

Tuesday, November 8, 2011

Registration	7:00am - 6:00pm	Gateway Foyer
Speaker's Breakfast	7:30 - 8:30am	Donner/Siskiyou Ballroom
AV Practice Rooms	7:00am - 6:00pm	Chardonnay, Riesling, Zinfandel

	Oak Ballroom	Fir Ballroom	Pine Ballroom	Cedar Ballroom
8:30 AM — TO — 10:00 AM	**Special Session 3** Emerging Technologies: The Next Logic Switch	**Session 4A** Advances in Global Routing	**Designer Track 1** Analog/Mixed-Signal Design Challenges: Temperature, Verification and the Human Factor	
	Coffee Break - Gateway Foyer			
10:30 AM — TO — 12:00 PM	**Tutorial 2** Nano-Electro-Mechanical Relay Integrated Circuits and Technology	**Session 5A** Routing Optimization Techniques	**Designer Track 2** Let's Gap Together! Urgent to do's for EDA from Industry Point of View	**Session 5C** System Level Modeling for Early Design Space Exploration, Simulation, and Synthesis
	Lunch - Watts Next... Speaker: Chris A. Malachowsky - NVIDIA Corp. **Donner/Siskiyou Ballroom**			Sponsored By: CEDA IEEE Council on Electronic Design Automation
1:30 PM — TO — 3:30 PM	**Session 6A** Modeling of Devices and Analog Systems	**Session 6B** Logic Level Synthesis	**Session 6C** Robustness and Variability	**Session 6D** CAD for Bio/Nano/Post-CMOS Systems
	Coffee Break - Gateway Foyer			
4:00 PM — TO — 6:00 PM	**Special Session 4** The Future of Clock Network Synthesis	**Session 7A** Analog Circuit Sizing and Layout Optimization	**Session 7B** Modeling and Simulation of Interconnect and Power Networks	**Session 7C** Stress, Electromigration, and Soft Error Mitigation
	6:30 - 8:45pm - EDA Consortium & IEEE Council on EDA 2011 Phil Kaufman Award Dinner **Donner/Siskiyou Ballroom** ** Special Registration Required**			

Wednesday, November 9, 2011

Registration	7:00am - 4:00pm	Gateway Foyer
Speaker's Breakfast	7:30 - 8:30am	Donner/Siskiyou Ballroom
AV Practice Rooms	7:00am - 4:00pm	Chardonnay, Riesling, Zinfandel

	Oak Ballroom	Fir Ballroom	Pine Ballroom	Cedar Ballroom
8:30 AM — TO — 10:00 AM	**Special Session 5** *Brain-Inspired Architectures: Abstractions to Accelerators*	**Session 8B** *Advances in Debugging and Simulation*	**Session 8C** *System-level Power Management*	
	Coffee Break - Gateway Foyer			
10:30 AM — TO — 12:30 PM	**Special Session 6** *2011 TAU Power Grid Simulation Contest*	**Session 9A** *Advances in Clocking and Routing for ASIC and On-Chip Communication*	**Session 9B** *Frontiers in Verification*	**Session 9C** *System-level Power and Thermal Estimation*
	Lunch - Donner/Siskiyou Ballroom			
2:00 PM — TO — 4:00 PM	**Tutorial 3** *Emerging Nonvolatile Memory and Memristors*	**Session 10A** *Advanced Timing and Power Optimizations in Physical Design*	**Session 10B** *Test Cost and Quality*	**Session 10C** *New Techniques for System-level Communication Synthesis and Hardware Metering*
	Coffee Break - Gateway Foyer			

4:30-5:30pm | PANEL: *Manycore, Heterogeneous, or Neither: Which One is the Way to Go for EDA?* **- Oak/Fir Ballroom**

Thursday, November 10, 2011

	Registration	*7:30am - 1:00pm*	*Gateway Foyer*	
	Oak Ballroom	**Fir Ballroom**	**Pine Ballroom**	**Cedar Ballroom**
8:30 AM — TO — 5:00 PM	***Workshop 1*** *IEEE/ACM Workshop on Variability Modeling and Characterization*	***Workshop 2*** *International Workshop on Adaptive Power Management with Machine Intelligence*	***Workshop 3*** *Seventh International Workshop on Constraints in Formal Verification (CFV'11)*	***Workshop 4*** *Nanolithography & IC Design/ CAD in Extreme Scaling: What, Why, and How?*
	11:00am - 1:00pm	*Workshop Lunch*	*Donner Ballroom*	
CANDE	*8:00am - 6:00pm*	*2011 CANDE Workshop*	*Siskiyou Ballroom*	

Opening Session & Keynote Address

9:00 - 10:30am • Oak/Fir Ballroom

OPENING REMARKS

Joel Phillips - **General Chair** - *Cadence Research Labs*

AWARD PRESENTATIONS

IEEE/ACM William J. McCalla ICCAD Best Paper Award

This award is given in memory of William J. McCalla for his contributions to ICCAD and his CAD technical work throughout his career.

9B.1 FORMAL VERIFICATION OF PHASE-LOCKED LOOPS USING REACHABILITY ANALYSIS AND CONTINUIZATION

Matthias Althoff, Akshay Rajhans, Bruce Krogh, Soner Yaldiz, Xin Li, Larry Pileggi - *Carnegie Mellon Univ.*

10A.1 GATE SIZING AND DEVICE TECHNOLOGY SELECTION ALGORITHMS FOR HIGH-PERFORMANCE INDUSTRIAL DESIGNS

Mustafa Ozdal, Steven Burns - *Intel Corp.*
Jiang Hu - *Texas A&M Univ.*

ICCAD Ten Year Retrospective Most Influential Paper Award

This award is being given to the paper judged to be most influential on research and industrial practice in computer-aided design of integrated circuits over the ten years since its original appearance at ICCAD.

2001 PAPER TITLED: EFFICIENT CONFLICT DRIVEN LEARNING IN BOOLEAN SATISFIABILITY SOLVER

Lintao Zhang - *Microsoft Corp.*
Conor Madigan – *Kateeva, Inc.*
Matthew Moskewicz - *Univ. of California, Berkeley*
Sharad Malik - *Princeton Univ.*

IEEE CEDA Early Career Award

Valeria Bertacco - *University of Michigan, Ann Arbor*
For outstanding contributions to hardware verification, including her work on semi-formal verification, runtime and post-silicon verification, and correctness-constrained execution.

2011 SIGDA Pioneering Achievement Award

Robert Brayton - *Univ. of California, Berkeley*
For outstanding contributions to the field of Computer Aided Design of integrated systems over the last several decades.

The CADathlon at ICCAD

Introduction of the 2011 winners.

KEYNOTE

Room: Oak/Fir Ballroom **9:00 - 10:30am**

Design of Secure Systems - Where are the EDA Tools?

Georg Sigl - *Technische Univ. München and Fraunhofer AISEC*
Email: sigl@tum.de or georg.sigl@aisec.fraunhofer.de

The design of security controllers, or more generally of microcontroller platforms implementing measures against hardware attacks, is still a very tedious handwork. Standardized and broadly available design tools as well as the necessary knowledge are rarely available and make secure hardware design a black art, known only within specialized companies building smart cards or Pay TV chips, for example. Secure hardware is, however, of increasing importance in many future embedded systems connected to cyber physical systems. Secure elements, i.e. special security chips or cores on a system on chip, are needed everywhere to protect these systems against physical attacks.

Within this talk, the speaker will give some insight in the design flow of two security controller platforms and the special challenges encountered there. After summarizing the main attack scenarios for security hardware, a selection of countermeasures will be presented. These countermeasures have to be implemented and verified during various phases in the design flow. Some self-made tools and scripts have been used to achieve the result of a highly secure implementation, but there is a huge opportunity to accelerate implementation and verification steps. Furthermore, the knowledge about security could be captured inside tools and relieve designers of the task of becoming hardware security experts.

The talk should motivate researchers in the EDA world to participate in the development of a new state-of-the-art design flow for secure hardware.

Georg Sigl finished his PhD in Electrical Engineering at TU München in 1992 in the area of layout synthesis. Afterwards he introduced new design-for-testability concepts in telecommunication ASICs at Siemens. In 1996 he joined the automotive microcontroller department at Siemens HL (later Infineon) to develop a universal library for peripherals to be used in 16- and 32-bit microcontrollers. From 2000 he was responsible for the development of new secure microcontroller platforms in the Chip Card and Security division. Under his responsibility, two award winning platforms - the SLE88 (Cartes Sesames Award 2001) and the SLE78 (Cartes Sesames Award 2008; Innovation Award of the German Industry 2010) - have been designed. In June 2010, he founded a new institute at Technical University Munich for Security in Electrical Engineering and Information Technology. In parallel, he is driving embedded security research as deputy director at the Fraunhofer Research Institution for Applied and Integrated Security AISEC Munich.

TUTORIAL

1T Room: Oak Ballroom 11:00am - 12:30pm

GPU Programming for EDA with OpenCL

ORGANIZER(S):

Rasit O. Topaloglu - *GLOBALFOUNDRIES*

SPEAKER(S):

Rasit O. Topaloglu - *GLOBALFOUNDRIES*
Benedict Gaster - *Advanced Micro Devices, Inc.*

Graphical processing unit (GPU) computing has been an interesting area of research in the last few years. While initial adapters of the technology have been from image processing domain due to difficulties in programming the GPUs, research on programming languages made it possible for people without the knowledge of low-level programming languages such as OpenGL develop code on GPUs.

Two main GPU architectures from AMD (former ATI) and NVIDIA acquired grounds. AMD adapted Stanford's Brook language and made it into an architecture-agnostic programming model. NVIDIA, on the other hand, brought CUDA framework to a wide audience. While the two languages have their pros and cons, such as Brook not being able to scale as well and CUDA having to account for architectural-level decisions, it has not been possible to compile one code on another architecture or across platforms.

Another opportunity came with the introduction of the idea of combining one or more CPUs and GPUs on the same die. Eliminating some of the interconnection bandwidth issues, this combination makes it possible to offload tasks with high parallelism to the GPU. The technological direction towards multicores for CPU-only architectures also require a programming methodology change and act as a catalyst for suitable programming languages. Hence, a unified language that can be used both on multiple core CPUs as well as GPUs and their combinations has gained interest. Open Computing Language (OpenCL), developed originally by the Khronos Group of Apple and supported by both AMD and NVIDIA, is seen as the programming language of choice for parallel programming. In this paper, we provide an introduction to OpenCL. We also use EDA as our application domain to get the readers started with programming the language of parallelism, OpenCL.

SESSION

1A Room: Fir Ballroom 11:00am - 12:30pm

Beyond Printing Single

MODERATOR(S):

Andres Torres - *Mentor Graphics Corp.*

This short session discusses multiple patterning and its interaction with physical design. The first paper presents one of the first methods for layout decomposition for triple patterning and also offers semi-definite programming based scalable heuristic for the same. The second paper shows that stitch minimization problem for double patterning is in P and gives an layout decomposition algorithm to minimize number of stitches optimally. The last paper offers a fast O(n) solution to the layout decomposition problem for double patterning and proposes a layout compaction method to fix double patterning conflicts.

1A.1* **LAYOUT DECOMPOSITION FOR TRIPLE PATTERNING LITHOGRAPHY**
Bei Yu, Boyang Zhang, Duo Ding, David Z. Pan - *Univ. of Texas, Austin*
Kun Yuan - *Cadence Design Systems, Inc.*

1A.2 **OPTIMAL LAYOUT DECOMPOSITION FOR DOUBLE PATTERNING TECHNOLOGY**
Minsik Cho - *IBM Corp.*
Xiaoping Tang - *Google, Inc.*

1A.3 **A FRAMEWORK FOR DOUBLE PATTERNING-ENABLED DESIGN**
Rani S. Ghaida, Puneet Gupta - *Univ. of California, Los Angeles*
Kanak Agarwal, Sani Nassif, Xin Yuan, Lars Liebmann - *IBM Corp.*

SESSION 1B

Room: Pine Ballrom **11:00am - 12:30pm**

Memory and Delay Test

MODERATOR(S):

Haralampos Stratigopoulos - *TIMA Laboratory/CNRS*

This session covers topics in memory and delay testing. The first paper introduces a new error correction code to improve memory reliability in the context of multimedia applications. The second paper discusses testing of extremely-low-voltage memory. The third paper presents a new efficient way to perform pseudo-functional testing for small delay defects.

1B.1 UNEQUAL ERROR PROTECTION CODES IN SRAMS FOR MOBILE MULTIMEDIA APPLICATIONS

Xuebei Yang - *Rice Univ.*

Kartik Mohanram - *Univ. of Pittsburgh*

1B.2 DETECTING STABILITY FAULTS IN SUB-THRESHOLD SRAMS

Chen-Wei Lin, Hao-Yu Yang, Chin-Yuan Huang, Hung-Hsin Chen, Mango C.T. Chao - *National Chiao Tung Univ.*

1B.3 PSEUDO-FUNCTIONAL TESTING FOR SMALL DELAY DEFECTS CONSIDERING POWER SUPPLY NOISE EFFECTS

Qiang Xu, Feng Yuan, Xiao Liu - *The Chinese Univ. of Hong Kong*

SESSION 1C

Room: Cedar Ballroom **11:00am - 12:30pm**

Manufacturing-Aware Optimizing Power, Performance and Reliability of the Memory Hierarchy of Embedded Systems

MODERATOR(S):

Puneet Gupta - *Univ. of California, Los Angeles*

Designing the memory hierarchy is a crucial step in the embedded system design workflow as it has a significant impact on the system's power and performance. The papers of this session address three different, but equally important aspects of memory design: power, performance and reliability.The first paper inspects the memory power profile of a video processing application and proposes using a multiple-sleep state model to improve power efficiency without sacrificing performance. The second paper leverages several new memory device technologies to create a hybrid memory hierarchy that is optimized for the bandwidth demands of an application. The last paper in the session proposes a control theory centric approach to improve transient error resilience in shared caches while satisfying performance goals.

1C.1 A LOW-POWER MEMORY ARCHITECTURE WITH APPLICATION-AWARE POWER MANAGEMENT FOR MOTION & DISPARITY ESTIMATION IN MULTIVIEW VIDEO CODING

Muhammad Shafique, Bruno Zatt, Jörg Henkel - *Karlsruher Institut für Technologie*

Sergio Bampi - *Univ. Federal do Rio Grande do Sul*

1C.2 BANDWIDTH-AWARE RECONFIGURABLE CACHE DESIGN WITH HYBRID MEMORY TECHNOLOGIES

Jishen Zhao, Cong Xu, Yuan Xie - *Pennsylvania State Univ.*

1C.3 FEEDBACK CONTROL BASED CACHE RELIABILITY ENHANCEMENT FOR EMERGING MULTICORES

Hui Zhao, Akbar Sharifi, Shekhar Srikantaiah, Mahmut Kandemir - *Pennsylvania State Univ.*

SPECIAL SESSION

1S

Room: Oak Ballroom 2:00 - 4:00pm

The ABCs of Formal Verification: Models, Algorithms, and Methodologies in RTL- and ESL-based Design Flows

MODERATOR(S):

Robert K. Brayton - *Univ. of California, Berkeley*

ORGANIZER(S):

Wolfgang Kunz - *Technische Universität Kaiserslautern*

This session reviews the scientific foundations of modern formal verification methods and their use in RTL- and ESL-based design flows. An overview of the basic proving techniques is presented and their characteristics in different applications are discussed. It will be demonstrated how basic algorithmic issues and the choice of computational models influences industrial verification methodologies. The tutorial reviews different coverage metrics for verification and their possible role in industrial flows.

ESL-based design flows pose new challenges for formal verification. We summarize the state-of-the-art in high-level equivalence checking and develop future perspectives of property checking in system-level design.

1S.1 THE FIRST TASTE OF FORMAL VERIFICATION
Alan Mishchenko - *Univ. of California, Berkeley*

1S.2 METHODOLOGIES OF SYSTEM-ON-CHIP PROPERTY CHECKING
Wolfgang Kunz - *Technische Universität Kaiserslautern*

1S.3 MEASURING VERIFICATION PROGRESS AND QUALITY
Raik Brinkmann - *OneSpin Solutions*

1S.4 SYSTEM-LEVEL TO RTL EQUIVALENCE CHECKING
Alfred Koelbl - *Synopsys, Inc.*

SESSION

2A

Room: Fir Ballroom 2:00 - 4:00pm

Placement and Clocking

MODERATOR(S):

Saurabh Adya - *Magma Design Automation, Inc.*
Joe Shinnerl - *Mentor Graphics Corp.*

Three papers in this session describe successful entries in the ISPD 2011 contest on routability-driven placement, held by IBM Research. They pursue different algorithmic techniques, but evaluate results on the same set of newly released industry benchmarks, facilitating direct comparisons. The fourth paper develops a methodology for optimizing placement and clocking with pulsed latches.

2A.1* A SIMPLR METHOD FOR ROUTABILITY-DRIVEN PLACEMENT
Jin Hu, Myung-Chul Kim, Dong-Jin Lee, Igor L. Markov - *Univ. of Michigan*

2A.2 RIPPLE: AN EFFECTIVE ROUTABILITY-DRIVEN PLACER BY ITERATIVE CELL MOVEMENT
Xu He, Tao Huang, Linfu Xiao, Haitong Tian, Guxin Cui, Evangeline F.Y. Young - *The Chinese Univ. of Hong Kong*

2A.3 ROUTABILITY-DRIVEN ANALYTICAL PLACEMENT FOR MIXED-SIZE CIRCUIT DESIGNS
Meng-Kai Hsu, Sheng Chou, Tzu-Hen Lin, Yao-Wen Chang - *National Taiwan Univ.*

2A.4 PRICE: POWER REDUCTION BY PLACEMENT AND CLOCK-NETWORK CO-SYNTHESIS FOR PULSED-LATCH DESIGNS
Yi-Lin Chuang, Yao-Wen Chang - *National Taiwan Univ.*
Hong-Ting Lin, Tsung-Yi Ho - *National Cheng Kung Univ.*
Diana Marculescu - *Carnegie Mellon Univ.*

SESSION 2B

Room: Pine Ballrom | 2:00 - 4:00pm

Recent Advances in Behavioral Modeling and Timing Analysis

MODERATOR(S):

Tao Lin - *Magma Design Automation, Inc.*
Xin Li - *Carnegie Mellon Univ.*

This session covers several recent advances in behavioral modeling and timing analysis. The first paper presents a novel technique for nonlinear macromodeling for analog circuits. The second paper proposes an elegant theoretical framework for optimal chip disposition. This work aims to find the best criterion to determine whether a chip is good or bad during production test. The last two papers focus on statistical timing analysis with consideration of large-scale temperature variations and post-silicon tunable clock buffers respectively.

2B.1 EFFICIENT ANALYTICAL MACROMODELING OF LARGE ANALOG CIRCUITS BY TRANSFER FUNCTION TRAJECTORIES
Dimitri De Jonghe, Georges Gielen - *Katholieke Univ. Leuven*

2B.2* OPTIMAL STATISTICAL CHIP DISPOSITION
Vladimir Zolotov, Jinjun Xiong - *IBM T.J. Watson Research Ctr.*

2B.3 TEMPERATURE AWARE STATISTICAL STATIC TIMING ANALYSIS
Artem Rogachev, Lu Wan, Deming Chen - *Univ. of Illinois at Urbana-Champaign*

2B.4 FAST STATISTICAL TIMING ANALYSIS FOR CIRCUITS WITH POST-SILICON TUNABLE CLOCK BUFFERS
Bing Li, Ning Chen, Ulf Schlichtmann - *Technische Univ. München*

SESSION 2C

Room: Cedar Ballroom | 2:00 - 4:00pm

Caches and Parallel Embedded Software

MODERATOR(S):

Nalini Vasudenvan - *Intel Corp.*

This long session addresses various aspects of embedded software, especially regarding parallelism. The first paper aims to improve the performance of shared caches by changing the layout of memory for object-oriented programs. The second proposes to more efficiently simulate a variety of cache configurations by understanding when the presence of data in one cache implies it in a second. The third proposes a technique for improving the performance of parallel programs by adding a thread that pre-analyzes data to better work on it in parallel. The fourth (short) paper consider better data layouts to improve cache behavior. The fifth (short) paper considers replicating critical instructions to harden programs against soft errors.

2C.1* IMPROVING SHARED CACHE BEHAVIOR OF MULTITHREADED OBJECT-ORIENTED APPLICATIONS IN MULTICORES
Mahmut Kandemir, Shekhar Srikantaiah - *Pennsylvania State Univ.*
Seung Woo Son - *Argonne National Lab*

2C.2 CIPARSIM: CACHE INTERSECTION PROPERTY ASSISTED RAPID SINGLE-PASS FIFO CACHE SIMULATION TECHNIQUE
Mohammad Shihabul Haque, Jorgen Peddersen, Sri Parameswaran - *Univ. of New South Wales*

2C.3 COOPERATIVE PARALLELIZATION
Praveen Yedlapalli, Emre Kultursay, Mahmut Kandemir - *Pennsylvania State Univ.*

2C.4S OPTIMIZING DATA LOCALITY USING ARRAY TILING
Mahmut Kandemir, Wei Ding, Yuanrui Zhang, Jun Liu - *Pennsylvania State Univ.*

2C.5S ASSURING APPLICATION-LEVEL CORRECTNESS AGAINST SOFT ERRORS
Karthik Gururaj, Jason Cong - *Univ. of California, Los Angeles*

SPECIAL SESSION

2S Room: Oak Ballroom 4:30 - 6:00pm

The Role of EDA in Digital Print Automation and Infrastructure Optimization

MODERATOR(S):

Mehdi Tahoori - *Karlsruher Institut für Technologie*

ORGANIZER(S):

Krishnendu Chakrabarty - *Duke Univ.*
Jun Zeng - *Hewlett-Packard Co.*

This session highlights the key role that EDA can play in the maturation of the digital print automation field. ICCAD attendees will learn about the basic concepts of digital printing, the application of discrete-event simulation to policy management and performance evaluation, and workplace design, resource management, and dynamic reconfiguration using EDA flows based on scheduling, resource binding, and physical design. EDA researchers will be exposed to an emerging technology that can benefit from a fresh EDA perspective on system design and optimization. It describes how the synergies between these fields can be exploited to not only benefit digital printing, but also to create new opportunities for EDA researchers and practitioners.

2S.1 A TUTORIAL ON DIGITAL PRINT TECHNOLOGY
Rick Bellamy - *Reischling Press, Inc.*

2S.2 A SIMULATION FRAMEWORK AND PLATFORM FOR DIGITAL PRINT
Gary Dispoto - *Hewlett-Packard Co.*

2S.3 A SYNTHESIS APPROACH FOR PRODUCTIVITY OPTIMIZATION IN DIGITAL PRINT AUTOMATION
Krishnendu Chakrabarty - *Duke Univ.*

SESSION

3A Room: Fir Ballroom 4:30 - 6:00pm

DFM: From Test Structures to Computation

MODERATOR(S):

Rasit Topaloglu - *GLOBALFOUNDRIES*

This short session discusses DFM approaches for variation characterization, modeling and simulation. The first paper proposes a sparse regression based technique to accurately decompose process variation into spatially correlated variation, and uncorrelated random variation components. The second paper presents two embedded test structures for carrying out path delay measurement in actual product designs. The third paper discuss two GPU-based aerial image simulation algorithms leveraging polygon-based convolution.

3A.1 TOWARD EFFICIENT SPATIAL VARIATION DECOMPOSITION VIA SPARSE REGRESSION
Wangyang Zhang, Xin Li - *Carnegie Mellon Univ.*
Karthik Balakrishnan, Duane Boning - *Massachusetts Institute of Technology*
Rob Rutenbar - *Univ. of Illinois at Urbana-Champaign*

3A.2 REBEL AND TDC: TWO EMBEDDED TEST STRUCTURES FOR ON-CHIP MEASUREMENTS OF WITHIN-DIE PATH DELAY VARIATIONS
Charles Lamech, James Aarestad, Jim Plusquellic, Reza Rad - *Univ. of New Mexico*
Kanak Agarwal - *IBM Corp.*

3A.3S ACCELERATING AERIAL IMAGE SIMULATION WITH GPU
Hongbo Zhang, Martin D.F. Wong, Sanjay J. Patel - *Univ. of Illinois at Urbana-Champaign*
Tan Yan - *Synopsys, Inc.*

SESSION 3B

Room: Pine Ballrom **4:30 - 6:00pm**

High-Level and Sequential Synthesis

MODERATOR(S):

Forrest Brewer - *Univ. of California, Santa Barbara*

This session describes effective practical work in classical high-level synthesis applications as well as a new approach for sequential synthesis to system aims. In the first paper, a simple combined approach for buffer allocation is mated with loop transformations to directly reduce off-chip communications. The second paper optimizes high-level design partitioning with controller and register binding to effectively limit the worst-case timing delays. In the third paper, a new approach for efficient parallel binary sequence generation is described. Such sequencers play a crucial role in system synthesis.

3B.1 COMBINED LOOP TRANSFORMATION AND HIERARCHY ALLOCATION FOR DATA REUSE OPTIMIZATION

Peng Zhang, Jason Cong, Yi Zou - *Univ. of California, Los Angeles*

3B.2 HIGH LEVEL SYNTHESIS WITH DISTRIBUTED CONTROLLERS FOR FAST TIMING CLOSURE

Seokhyun Lee, Kiyoung Choi - *Seoul National Univ.*

3B.3 SYNTHESIS OF PARALLEL BINARY MACHINES

Elena Dubrova - *Royal Institute of Technology*

SESSION 3C

Room: Cedar Ballroom **4:30 - 6:00pm**

Addressing the Physical Challenges of NoC Design

MODERATOR(S):

Sherief Reda - *Brown Univ.*

The introduction of many-core processors and 3D integration motivate the need for sophisticated NoC design techniques. This session has three papers that address important considerations in NoC designs, including performance, area, power, and reliability. The first paper proposes new techniques for designing NoCs that lead to improved chemical mechanical polishing in 3D ICs. The second paper proposes new routing techniques to avoid deadlocks in mesh NoC. The third paper analyzes the power-performance-area trade-offs of a number of different NoC designs.

3C.1 CHEMICAL-MECHANICAL POLISHING AWARE APPLICATION-SPECIFIC 3D NOC DESIGN

Wooyoung Jang, Jae-Seok Yang, *Samsung*
David Z. Pan - *Univ. of Texas, Austin*
Ou He - *IBM Systems and Technology Group*

3C.2 APPLICATION-AWARE DEADLOCK-FREE OBLIVIOUS ROUTING BASED ON EXTENDED TURN-MODEL

Ali Shafiee, Mahdy Zolghadr, Mohammad Arjomand, Hamid Sarbazi-Aazd - *Sharif Univ. of Technology*

3C.3 CO-DESIGN OF CHANNEL BUFFERS AND CROSSBAR ORGANIZATIONS IN NOCS ARCHITECTURES

Avinash Kodi, Randy Morris, Dominic Ditomaso - *Ohio Univ.*
Ashwini Sarathy, Ahmed Louri - *Univ. of Arizona*

PANEL

1P Room: Oak/Fir Ballroom 6:30 - 7:30pm

2020 Vision: What the Recent History of EDA will Look Like in Nine Years

MODERATOR(S):

William Joyner - *Semiconductor Research Corporation*

ORGANIZER(S):

Helmut Graeb - *Technische Univ. München*

PANELIST(S):

Patrick Groeneveld - *Magma Design Automation, Inc.*
Thomas Harms - *IEEE CEDA and Infineon*
Pei-Hsin Ho - *Synopsys, Inc.*
Suk Lee - *Taiwan Semiconductor Manufacturing Co., Ltd.*
Sani Nassif - *IBM Corp.*
Nobuyuki Nishiguchi - *Semiconductor Technology Academic Research Center*

Panels on the history of EDA are often entertaining, because there are actual stories of real events - successes and failures. But this panel is more difficult, because our panelists will be asked about the future. Where will EDA be in 2020? Will we still be going down the Moore's Law curve, enabling design in a 4nm technology? Will we still be talking about "More Moore" and "More than Moore" or something between or entirely beyond? How many EDA tools/vendors will be needed to design a system on chip? Will we finally be at the point where applications, rather than technology progress, are driving research? Will researchers still be publishing papers showing 5% improvements in techniques that do the same things as today, or will there be new and exciting challenges continuing to attract the best minds we have?

The panelists will address these questions from their own perspectives and the audience will participate in supporting (or disputing) their views!

Room: Donner/Siskiyou Ballroom 7:30 - 9:00pm

ACM/SIGDA Member Meeting

The annual ACM/SIGDA Member Meeting is open to all members of the EDA community.

This meeting will feature an informal talk by the SIGDA Pioneering Achievement award recipient. This year, the award will be presented to Prof. Robert K. Brayton of UC Berkeley, in recognition of his contributions to a wide range of EDA research areas.

Everyone is invited to join the meeting for a light dinner, refreshments, and an entertaining and interesting talk.

For more information, please visit www.sigda.org/pioneer.

2011 SIGDA Pioneering Achievement Award Recipient:

For outstanding contributions to the field of Computer Aided Design of integrated systems over the last several decades.

Robert Brayton, Univ. of California, Berkeley

Please join us!

SPECIAL SESSION

3S | Room: Oak Ballroom | 8:30 - 10:00am

Emerging Technologies: The Next Logic Switch

ORGANIZER(S):

Mehdi Tahoori - *Karlsruher Institut für Technologie*

Major challenges looming over the future of the semiconductor industry include power and performance optimization; interconnects; device fabrication; faults and defects; fabline cost; and control of variations at the nanoscale; and, integration of a diverse set of materials and devices on the same chip.

There are a number of promising emerging devices that can be considered for future electronics. Examples include carbon nanotube field effect transistors (CNTFETs), carbon interconnects, nanowires, and Bilayer PseudoSpin Field-Effect Transistor (BiSFET). The objective of this special session is to bring the attention of design automation community to these novel devices, including the challenges and opportunities.

3S.1 CARBON NANOTUBE IMPERFECTION-IMMUNE DIGITAL VLSI: FREQUENTLY ASKED QUESTIONS UPDATED
Subhasish Mitra, Hai Wei, Jie Zhang, Nishant Patel, Albert Lin, Max M. Shulaker, Hong-Yu Chen, H.-S. Philip Wong - *Stanford Univ.*
Lan Wei - *Massachusetts Institute of Technology*

3S.2 ALTERNATIVE DESIGN METHODOLOGIES FOR THE NEXT GENERATION LOGIC SWITCH
Giovanni DeMicheli, Davide Sacchetto, Michele De Marchi, Yusuf Leblebici - *Ecole Polytechnique Fédérale de Lausanne*

3S.3 A PROPOSED NOVEL GRAPHENE SWITCH: BILAYER PSEUDOSPIN FIELD EFFECT TRANSISTOR
Sanjay Banerjee, Frank Register, Emanuel Tutuc - Univ. of Texas, Austin

SESSION

4A | Room: Fir Ballroom | 8:30 - 10:00am

Advances in Global Routing

MODERATOR(S):

Zhuo Li - *IBM Corp.*
Yi-Kan Cheng - *Taiwan Semiconductor Manufacturing Co., Ltd.*

The three papers in this session deal with the global routing problem. The first paper uses a multi-level rerouting framework on a 3D routing grid to achieve high quality routing solutions. The second paper presents a parameterized integer programming model to quickly identify congestion hotspots for a small analysis time-budget. The third paper considers global routing in the context of multiple power domains to avoid routing through domains that may be shut down.

4A.1* MGR: MULTI-LEVEL GLOBAL ROUTER
Yue Xu - *Iowa State Univ. and Cadence Design Systems, Inc.*
Chris Chu - *Iowa State Univ.*

4A.2 CONGESTION ANALYSIS FOR GLOBAL ROUTING VIA INTEGER PROGRAMMING
Hamid Shojaei, Azadeh Davoodi, Jeffrey Linderoth - *Univ. of Wisconsin*

4A.3 HIGH-QUALITY GLOBAL ROUTING FOR MULTIPLE DYNAMIC SUPPLY VOLTAGE DESIGNS
Wen-Hao Liu, Yih-Lang Li - *National Chiao Tung Univ.*
Kai-Yuan Chao - *Intel Corp.*

DESIGNER TRACK

1 Room: Pine Ballrom 8:30 - 10:00am

Analog/Mixed-Signal Design Challenges: Temperature, Verification and the Human Factor

MODERATOR(S):

Lei He - *Univ. of California, Los Angeles*

ORGANIZER(S):

Helmut Graeb - *Technische Univ. München*

Experienced engineers from industry will talk about urgent problems in analog/mixed-signal design for system-on-chips. The first talk will deal with the problem of local heating in automotive SoCs, which can reach over 700K, and how to verify correct behavior using thermal simulation, placement information and static timing analysis. The second talk will cover the problem of efficient and systematic verification of analog/mixed-signal systems and outline gaps in today's verification flows. The third talk will discuss why analog design is still there, and why analog design automation has not been successful, and how it might become successful by incorporating the human factor.

4B.1 ASSESSING THE IMPACT OF STEEP TEMPERATURE GRADIENTS WITHIN AUTOMOTIVE POWER SOCS
Volker Meyer zu Bexten, Christian Funke, Jens Bargfrede - Infineon Technologies AG

4B.2 GAPS IN THE VERIFICATION OF AUTOMOTIVE MIXED-SIGNAL SYSTEMS
Achim Graupner - *ZMDI*

4B.3 THE HUMAN FACTOR IN MIXED-SIGNAL DESIGN AND ITS CONSEQUENCES FOR EDA
Ralf Brederlow - *Texas Instruments, Inc.*

TUTORIAL

2T

Room: Oak Ballroom **10:30am - 12:00pm**

Nano-Electro-Mechanical Relay Integrated Circuits and Technology

ORGANIZER(S):

Mehdi Tahoori - *Karlsruher Institut für Technologie*

SPEAKER(S):

Dejan Markovic - *Univ. of California, Los Angeles*
Vladimir Stojanovic - *Massachusetts Institute of Technology*
Elad Alon - *Univ. of California, Berkeley*

No matter how slowly they are allowed to run, digital logic gates implemented with CMOS transistors have a well-defined minimum energy that they must dissipate for each operation they perform. In contrast, switches based on mechanically making or breaking physical contact can achieve zero leakage and nearly infinite subthreshold slope, and hence may someday enable drastic reductions in energy. This potential has therefore driven significant recent interest and progress in integrated circuits and technology based on nano-electro-mechanical (NEM) relays. This tutorial provides a cross-cutting overview of recent research efforts to develop such a NEM relay technology.

SESSION

5A

Room: Fir Ballroom **10:30am - 12:00pm**

Routing Optimization Techniques

MODERATOR(S):

Mustafa Ozdal - *Intel Corp.*
Dwight Hill - *Synopsys, Inc.*

The four papers in this session address various issues in VLSI routing. The first paper addresses the issue of manufacturability by considering lithographic proximity and optical proximity correction simultaneously in the proposed gridless detailed router. The second paper proposes a jumper insertion algorithm that allows jumpers to be placed on any layer, taking into account both timing and antenna ratio constraints. The third paper accelerates global routing using a hybrid high throughput computing environment with both CPUs and GPUs. The fourth paper solves the escape routing problem for PCBs with staggered pin arrays with a linear program or an integer linear program formulation.

5A.1 DOPPLER: DPL-AWARE AND OPC-FRIENDLY GRIDLESS DETAILED ROUTING WITH MASK DENSITY BALANCING
Yen-Hung Lin, Yih-Lang Li - *National Chiao Tung Univ.*
Yong-Chan Ban, David Z. Pan - *Univ. of Texas, Austin*

5A.2 A JUMPER INSERTION ALGORITHM UNDER ANTENNA RATIO AND TIMING CONSTRAINTS
Luca Macchiarulo, Xin Gao - *Univ. of Hawaii*

5A.3S EXPLORING HIGH THROUGHPUT COMPUTING PARADIGM FOR GLOBAL ROUTING
Koushik Chakraborty, Yiding Han, Dean Michael Ancajas, Sanghamitra Roy - *Utah State Univ.*

5A.4S ESCAPE ROUTING FOR STAGGERED-PIN-ARRAY PCBS
Yuan-Kai Ho, Hsu-Chieh Lee, Yao-Wen Chang - *National Taiwan Univ.*

DESIGNER TRACK

2 Room: Pine Ballrom 10:30am - 12:00pm

Let's Gap Together! Urgent ToDo's for EDA from Industry Point of View

MODERATOR(S):

Yiyu Shi - *Missouri Univ. of Science and Technology*

ORGANIZER(S):

Helmut Graeb - *Technische Univ. München*

This session is dedicated to look at gaps in the CAD-supported design flow for integrated systems on chip. The major players Broadcom, Ericsson, Freescale, Hewlett Packard, IBM, Infineon, Intel, Maxim-IC, Oracle, and Texas Instruments have gathered in the Design Technology Committee to analyze urgent needs in implementation and verification of ICs and present them to the audience. Other issues in the 32 nm and below technology nodes are electromigration reliability and variability. We will hear how technology development, circuit design and CAD communities can jointly overcome this challenge.

5B.1 JOINT INDUSTRY EFFORT TO ADDRESS GAPS IN FUNCTIONAL VERIFICATION AND DIGITAL IMPLEMENTATION TOOLS

Matthias Bauer, Werner May, Thomas Harms - *Infineon Technologies*
Jay Bhadra, Bart Martinec, Bill Read - *Freescale Semiconductor, Inc.*
David Crohn, Jing Li, James You - *Broadcom Corp.*
Thomas Dillinger - *Oracle*
Björn Fjellborg - *Ericsson*
Joonyoung Kim, Ramond Rodriguez, Robert Titus - *Intel Corp.*
David Lacey, Hassan Naser, **Martin Foltin** - *Hewlett-Packard Co.*
Khankap Mounarath, Helen Xia - *Maxim Integrated Products, Inc.*
Arjun Rajagopal - *Texas Instruments, Inc.*
Shyam Ramji, Christopher J. Spandikow - *IBM Corp.*

5B.2 UNITING TO OVERCOME A MOUNTING BEOL ELECTROMIGRATION RELIABILITY CHALLENGE

Leon Sigal - *IBM T.J. Watson Research Ctr.*
C.K. Hu, S. Nassif - *IBM Research*
C. Xu, H. Smith, J. Wanock - *IBM Systems and Technology Group*

5B.3 HANDLING VARIABILITY IN BLOCK-LEVEL DESIGN - CHALLENGES & SOLUTIONS

Frank Schenkel - *MunEDA GmbH*

SESSION

5C Room: Cedar Ballroom 10:30am - 12:00pm

System Level Modeling for Early Design Space Exploration, Simulation, and Synthesis

MODERATOR(S):

Mahmut Kandemir - *Pennsylvania State Univ.*
Ken Stevens - *Univ. of Utah*

In the first presentation of this session the authors present a model of computational efficiency of ICs using either 2D or 3D processes. The model takes into account computational resources, interconnects, and memories, as well as power and thermal effects. The authors of the second paper present a model and simulation tool for analyzing the performance, area, and power consumption of spin-transfer torque RAM (STT-RAM). The basic idea of the last paper is to leverage the OpenCL parallel programming model for hardware modeling and synthesis. The authors present an automated methodology for mapping OpenCL applications to stream-based customizable hardware coprocessors targeted for FPGA implementation.

5C.1 MODELING THE COMPUTATIONAL EFFICIENCY OF 2-D AND 3-D SILICON PROCESSORS FOR EARLY-CHIP PLANNING

Matthew Grange, Dinesh Pamunuwa - *Lancaster Univ.*
Axel Jantsch - *KTH Royal Inst. of Tech.*
Roshan Weerasekera - *Agency for Science, Tech and Research*

5C.2 THE STETSIMS STT-RAM SIMULATION AND MODELING SYSTEM

Clint Smullen, Anurag Nigam, Sudhanva Gurumurthi, Mircea Stan - *Univ. of Virginia*

5C.3 MASSIVELY PARALLEL PROGRAMING MODELS USED AS HARDWARE DESCRIPTION LANGUAGES: THE OPENCL CASE

Muhsen Owaida, Nikolaos Bellas, Christos Antonopoulos, Konstantis Daloukas, Charalambos Antoniadis - *Univ. of Thessaly*

LUNCH PRESENTATION

Room: Donner/Siskiyou Ballroom 12:00 - 1:15pm

Watts Next...

SPEAKER(S):

Chris A. Malachowsky - *NVIDIA Corp.*

Making the most economical and efficient use of power for a processor is not just good for the environment, it is essential. In this talk I will discuss power efficiency as it applies across NVIDIA's broad range of processor offerings from supercomputers to cell phones.

Sponsored By:

CEDA
IEEE Council on Electronic Design Automation

SESSION 6A

Room: Oak Ballroom **1:30 - 3:30pm**

Modeling of Devices and Analog Systems

MODERATOR(S):

Amith Singhee - *IBM T.J. Watson Research Ctr.*
Luca Daniel - *Massachusetts Institute of Technology*

The papers in this session deal with various issues in modeling, ranging from handling variability to dealing with multi-domain systems. The first two papers discuss statistical modeling and efficient simulation techniques for device variability. The next two papers address order reduction of analog systems as well as specification and modeling of multi-domain dynamical systems.

6A.1 FAST STATISTICAL MODEL OF TIO2 THIN-FILM MEMRISTOR AND DESIGN IMPLICATION

Miao Hu, Hai Li - *Polytechnic Institute of New York Univ.*
Robinson E. Pino - *Air Force Research Laboratory/RITC*

6A.2 ACCELERATED STATISTICAL SIMULATION VIA ON-DEMAND HERMITE SPLINE INTERPOLATIONS

Rouwaida Kanj, Kanak Agarwal, Ali Sadigh, Sani Nassif - *IBM Research - Austin*
Tong Li, David Winston - *IBM Systems and Technology Group*
Rajiv Joshi - *IBM T.J. Watson Research Ctr.*

6A.3 STRUCTURE PRESERVING REDUCED-ORDER MODELING OF LINEAR PERIODIC TIME-VARYING SYSTEMS

Ting Mei, Heidi Thornquist, Eric Keiter, Scott Hutchinson - *Sandia National Laboratories*

6A.4 MODSPEC: AN OPEN, FLEXIBLE SPECIFICATION FRAMEWORK FOR MULTI-DOMAIN DEVICE MODELLING

David Amsallem, Jaijeet Roychowdhury - *Univ. of California, Berkeley*

SESSION 6B

Room: Fir Ballroom **1:30 - 3:30pm**

Logic Level Synthesis

MODERATOR(S):

Barry Pangrle - *Mentor Graphics Corp.*

In this session, novel directions vie with practical techniques for improving logic synthesis. The first paper describes a simple approach for AIG-based timing optimization. In the second paper, a SAT based incremental approach to design rectification for multiple errors is proposed. In the third paper, an efficient approach based on Craig Interpolation and SAT for automated decoder synthesis from bounded observations. In the fourth (short) paper, conventional approaches to logic synthesis are formally generalized for threshold logic applications. Finally, in the last (short) paper, an alternative approach for automated decoder synthesis is described.

6B.1 DELAY OPTIMIZATION USING SOP BALANCING

Alan Mishchenko, Robert Brayton - *Univ. of California, Berkeley*
Stephen Jang - *Agate Logic, Inc.*
Victor Kravets - *IBM Corp.*

6B.2 MATCH AND REPLACE-- A FUNCTIONAL ECO ENGINE FOR MULTI-ERROR CIRCUIT RECTIFICATION

Shao-Lun Huang, Wei-Hsun Lin, Chung-Yang Ric Huang - *National Taiwan Univ.*

6B.3 TOWARDS COMPLETELY AUTOMATIC DECODER SYNTHESIS

Jie-Hong Roland Jiang, Hsiou-Yuan Liu, Yen-Cheng Chou, Chen-Hsuan Lin - *National Taiwan Univ.*

6B.4S ON REWIRING AND SIMPLIFICATION FOR CANONICITY IN THRESHOLD LOGIC CIRCUITS

Ching-Yi Huang, Pin-Yi Kuo, Chun-Yao Wang - *National Tsing Hua Univ.*

6B.5S INFERRING ASSERTION FOR COMPLEMENTARY SYNTHESIS

Shengyu Shen, Ying Qin, Jianman Zhang - *National Univ. of Defense Technology*

SESSION 6C

Room: Pine Ballroom **1:30 - 3:30pm**

Robustness and Variability

MODERATOR(S):

Arijit Raychowdhury - *Intel Corp.*
Miroslav Velev - *Aries Design Automation, LLC*

This session covers topics ranging from variation analysis in digital and analog circuits, as well as, aging and dealing with timing violations. The first paper addresses the topic of variation-aware aging analysis in digital circuits, while the second targets stability analysis in analog circuits. The impact of NBTI induced aging on failure diagnosis is covered by the third paper. The last two papers address clock tuning for mitigating performance degradation or increasing performance.

6C.1 STATISTICAL AGING ANALYSIS WITH PROCESS VARIATION CONSIDERATION
Sangwoo Han, Joohee Choung, Juho Kim - *Sogang University*
Byung-Su Kim, Bong Hyun Lee, Hungbok Choi - *Samsung*

6C.2 A NEW METHOD FOR MULTIPARAMETER ROBUST STABILITY DISTRIBUTION ANALYSIS OF LINEAR ANALOG CIRCUITS
Changhao Yan, Xuan Zeng - *Fudan Univ.*
Sheng-Guo Wang - *Univ. of North Carolina, Charlotte*

6C.3 FAILURE DIAGNOSIS OF ASYMMETRIC AGING UNDER NBTI
Jyothi Bhaskarr Velamala, Venkatesa Ravi, Yu Cao - *Arizona State Univ.*

6C.4S IN-SYSTEM AND ON-THE-FLY CLOCK TUNING MECHANISM TO COMBAT LIFETIME PERFORMANCE DEGRADATION
Zahra Lak, Nicola Nicolici - *McMaster Univ.*

6C.5S ONLINE CLOCK SKEW TUNING FOR TIMING SPECULATION
Rong Ye, Feng Yuan, Qiang Xu - *The Chinese Univ. of Hong Kong*

SESSION 6D

Room: Cedar Ballroom **1:30 - 3:30pm**

CAD for Bio/Nano/Post-CMOS Systems

MODERATOR(S):

Deming Chen - *Univ. of Illinois at Urbana-Champaign, Urbana, Champaign*

This session has four interesting papers which cover different aspects of CAD for bio, nano, and post-CMOS systems. The first paper addresses the reliability issues for pin-constrained digital microfluidic biochips. The second paper is on defect-tolerant nanocrossbar implementation, through a novel approach with simultaneous mapping and morphing. The third and fourth papers are on spin-transfer torque random access memory (STT-RAM), an emerging and promising non-volatile memory, from device-architecture co-optimization and cell design optimization perspectives.

6D.1 RELIABILITY-ORIENTED BROADCAST ELECTRODE-ADDRESSING FOR PIN-CONSTRAINED DIGITAL MICROFLUIDIC BIOCHIPS
Tsung-Yi Ho, Tsung-Wei Huang - *National Cheng Kung Univ.*
Krishnendu Chakrabarty - *Duke Univ.*

6D.2 DEFECT-TOLERANT LOGIC IMPLEMENTATION ONTO NANOCROSSBARS BY EXPLOITING MAPPING AND MORPHING SIMULTANEOUSLY
Wenjing Rao, Yehua Su - *Univ. of Illinois*

6D.3 DEVICE-ARCHITECTURE CO-OPTIMIZATION OF STT-RAM BASED MEMORY FOR LOW POWER EMBEDDED SYSTEMS
Cong Xu, Dimin Niu, Yuan Xie - *Pennsylvania State Univ.*
Xiaochun Zhu, Seung H. Kang, Matt Nowak - *Pennsylvania State Univ. and Qualcomm, Inc.*

6D.4 STT-RAM CELL DESIGN OPTIMIZATION FOR PERSISTENT AND NON-PERSISTENT ERROR RATE REDUCTION: A STATISTICAL DESIGN VIEW
Yaojun Zhang, Yiran Chen - *Univ. of Pittsburgh*
Xiaobin Wang - *Seagate Technology*

SPECIAL SESSION

4S Room: Oak Ballroom 4:00 - 6:00pm

The Future of Clock Network Synthesis

MODERATOR(S):

Andrew B. Kahng - *Univ. of California at San Diego*

ORGANIZER(S):

Cliff Sze - *IBM Corp.*

The clock distribution network presents one of the most important design challenges in high-performance synchronous VLSI designs. However, automation in clock network synthesis is usually limited to local clock domains for two main reasons. (1) Global clock is too important for designers to take the risk of adopting a fully automated clocking flow. (2) Unlike in other EDA areas (such as placement/routing), clock synthesis tools are highly tied to clock network topologies, ground/power planning, clock gating, macro floorplanning, clocking methodologies, etc. It is thus very difficult to implement a set of generic clock synthesis tools for design productivity considerations. At the same time, Moore's Law scaling has led to more multi-core and system-on-a-chip designs in production; in this regime, clock network synthesis has become a major productivity showstopper. EDA vendors and design houses have recently observed new challenges in clock network synthesis automation and an urgent demand in generic clocking tools for performance, power, variability tolerance, and yield. The session includes a presentation from the winning team of the 2 ISPD clock network synthesis contests, along with two tutorials from industrial clocking experts discussing future challenges in clock distribution network design and automation.

4S.1 MYTH BUSTERS: MICROPROCESSOR CLOCKING IS FROM MARS, ASIC'S CLOCKING IS FROM VENUS?
Joseph Kozhaya - *IBM Corp.*
Philip Restle, Haifeng Qian - *IBM T.J. Watson Research Ctr.*

4S.2 CLOCKING DESIGN AUTOMATION IN INTEL'S CORE I7 AND FUTURE DESIGNS
Ali El-Husseini, Matthew Morrise - *Intel Corp.*

4S.3 ALGORITHMIC TUNING OF CLOCK TREES AND DERIVED NON-TREE STRUCTURES
Igor L. Markov, Dong-Jin Lee - *Univ. of Michigan*

SESSION

7A Room: Fir Ballroom 4:00 - 6:00pm

Analog Circuit Sizing and Layout Optimization

MODERATOR(S):

Lars Hedrich - *Frankfurt Univ.*

This session discusses recent progress in the optimization of the sizing and layout of analog circuits. The first paper presents a method for the efficient calculation of uniformly spread Pareto trade-off fronts for bicriterial designs. The second paper describes a methodology for the synthesis of local resonant clocks, which reduces clock power consumption. Two papers describe the use and extensions of B*-trees to accommodate typical constraints used in analog circuit layouts. Finally, the last paper present a fast prototyping method for layout migration of nanometer designs.

7A.1 PTRACE: DERIVATIVE-FREE LOCAL TRACING OF BICRITERIAL DESIGN TRADEOFFS
Amith Singhee - *IBM T.J. Watson Research Ctr.*

7A.2 A METHODOLOGY FOR LOCAL RESONANT CLOCK SYNTHESIS USING LC-ASSISTED LOCAL CLOCK BUFFERS
Walter Condley, Xuchu Hu, Matthew Guthaus - *Univ. of California, Santa Cruz*

7A.3 A CORNER STITCHING COMPLIANT B*-TREE REPRESENTATION AND ITS APPLICATIONS TO ANALOG PLACEMENT
Hui-Fang Tsao, Pang-Yen Chou, Shih-Lun Huang, Yao-Wen Chang - *National Taiwan Univ.*
Mark Po-Hung Lin - *National Chung Cheng Univ.*
Duan-Ping Chen - *Lattice Semiconductor Corp.*
Dick Liu - *Synopsys, Inc.*

7A.4S HETEROGENEOUS B*-TREES FOR ANALOG PLACEMENT WITH SYMMETRY AND REGULARITY CONSIDERATIONS
Hung-Chih Ou, Pang-Yen Chou, Yao-Wen Chang - *National Taiwan Univ.*

7A.5S FAST ANALOG LAYOUT PROTOTYPING FOR NANOMETER DESIGN MIGRATION
Po-Cheng Pan, Yi-Peng Weng, Hung-Ming Chen, Chien-Hung Chen, Wei-Zen Chen - *National Chiao Tung Univ.*
Tung-Chieh Chen - *SpringSoft, Inc.*

SESSION 7B

Room: Pine Ballroom — 4:00 - 6:00pm

Modeling and Simulation of Interconnect and Power Networks

MODERATOR(S):

Ibrahim (Abe) M. Elfadel - *Masdar Institute of Science and Tech.*

This session includes five papers on modeling, simulation and verification of interconnect and power networks. The first paper introduces a novel technique for model order reduction of dynamic systems with parameterized state and input/output matrices. The second and the fourth paper present two different preconditioning methods for fast iterative solution of large-scale power grids. The third paper introduces a mixed-integer linear programming algorithm for the estimation of power supply noise in digital circuits. The last paper proposes a vectorless verification scheme for RLC grids including transient current constraints.

7B.1* MODEL ORDER REDUCTION OF FULLY PARAMETERIZED SYSTEMS BY RECURSIVE LEAST SQUARE OPTIMIZATION
Zheng Zhang, Luca Daniel - *Massachusetts Institute of Technology*
Ibrahim (Abe) M. Elfadel - *Masdar Institute of Science and Tech.*

7B.2 FAST POISSON SOLVER PRECONDITIONED METHOD FOR ROBUST POWER GRID ANALYSIS
Jianlei Yang, Yici Cai, Qiang Zhou, Jin Shi - *Tsinghua Univ.*

7B.3 MODELING AND ESTIMATION OF POWER SUPPLY NOISE USING LINEAR PROGRAMMING
Farshad Firouzi, Saman Kiamehr, Mehdi Tahoori - *Karlsruher Institut für Technologie*

7B.4S POWER GRID ANALYSIS WITH HIERARCHICAL SUPPORT GRAPHS
Zhuo Feng, Xueqian Zhao, Jia Wang, Shiyan Hu - *Michigan Technological Univ.*

7B.5S VECTORLESS VERIFICATION OF RLC POWER GRIDS WITH TRANSIENT CURRENT CONSTRAINTS
Jia Wang, Xuanxing Xiong - *Illinois Institute of Technology*

SESSION 7C

Room: Cedar Ballroom — 4:00 - 6:00pm

Stress, Electromigration, and Soft Error Mitigation

MODERATOR(S):

Qiang Xu - *The Chinese Univ. of Hong Kong*
Yuan Xie - *Pennsylvania State Univ., State College*

This session addresses a variety of topics related to robustness of 2D and 3D integrated systems. The first two papers target 3D integrated circuits and their stress/electromigration characterization. In the same vein, but looking at 2D integrated systems, the third paper addresses the problem of variation-aware electromigration modeling of power ground networks. The last two papers target soft error mitigation in the context of multiple bit upsets in SRAMs and interconnect errors in FPGAs.

7C.1 ELECTROMIGRATION MODELING AND FULL-CHIP RELIABILITY ANALYSIS FOR BEOL INTERCONNECT IN TSV-BASED 3D ICS
Mohit Pathak, Sung Kyu Lim - *Georgia Institute of Technology*
Jiwoo Pak, David Z. Pan - *Univ. of Texas, Austin*

7C.2 FULL-CHIP THROUGH-SILICON-VIA INTERFACIAL CRACK ANALYSIS AND OPTIMIZATION FOR 3D IC
Moongon Jung, Xi Liu, Suresh K. Sitaraman, Sung Kyu Lim - *Georgia Institute of Technology*
David Z. Pan - *Univ. of Texas, Austin*

7C.3S VARIATION-AWARE ELECTROMIGRATION ANALYSIS OF POWER/GROUND NETWORKS
Di-An Li, Malgorzata Marek-Sadowska - *Univ. of California, Santa Barbara*

7C.4S LOW-POWER MULTIPLE-BIT UPSET TOLERANT MEMORY OPTIMIZATION
Seokjoong Kim, Matthew Guthaus - *Univ. of California, Santa Cruz*

7C.5S MITIGATING FPGA INTERCONNECT SOFT ERRORS BY IN-PLACE LUT INVERSION
Naifeng Jing, Weifeng He, Zhigang Mao - *Shanghai Jiao Tong Univ.*
Ju-Yueh Lee, Lei He - *Univ. of California, Los Angeles*

AWARD DINNER

Room: Donner/Siskiyou Ballroom **6:30 - 8:45pm**

EDA Consortium & IEEE CEDA 18th Annual Phil Kaufman Award Dinner

EDA Consortium and IEEE CEDA are hosting the Phil Kaufman dinner at the DoubleTree Hotel during the ICCAD Conference.

The Phil Kaufman Award honors individuals who have made an impact on the field of EDA and pays tribute to Phil Kaufman, the late industry pioneer who turned innovative technologies into commercial businesses that have benefited electronic designers.

Dr. C. L. David Liu, the William Mong honorary chair, professor of Computer Science and former president of the National Tsing Hua University in Hsinchu, Taiwan, will be presented with this year's Phil Kaufman Award for Distinguished Contributions to Electronic Design Automation (EDA).

******Special Registration is Required******

Co-Sponsors

CEDA IEEE Council on Electronic Design Automation

EDA CONSORTIUM

SPECIAL SESSION

5S Room: Oak Ballroom 8:30 - 10:00am

Brain-Inspired Architectures: Abstractions to Accelerators

ORGANIZER(S):

Yuan Xie - *Pennsylvania State Univ.*

Understanding the brain is one of the grand challenges in science and technology. Beyond gaining insights towards reverse engineering the brain for the design of next-generation robust and energy-efficient computer systems, understanding the brain can help develop medical interventions to address brain health. System designers and CAD researchers through contributions to abstraction models, design exploration frameworks and computational accelerators can help accomplishing this grand challenge. This special session will have three team talks (to emphasize the cross-disciplinary efforts) that cover recent progress in this direction in the system design and CAD community and help identify outstanding challenges.

5S.1 NEUROMORPHIC MODELING ABSTRACTIONS AND SIMULATION OF LARGE-SCALE CORTICAL NETWORKS

Jeffrey L. Krichmar, Nikil Dutt - *Univ. of California, Irvine*
Jayram M. Nageswaran, Micah Richert - *Brain Corp.*

5S.2 A FPGA-BASED CAD FRAMEWORK FOR EXPLORING NEUROMORPHIC VISION ALGORITHMS

Chaitali Chakrabarti, C-L. Yu - *Arizona State Univ.*
M. Debole, A. Al Maashri, M. Cotter, **Vijaykrishnan Narayanan** - *Pennsylvania State Univ.*

5S.3 A HETEROGENEOUS ACCELERATOR PLATFORM FOR MULTI-SUBJECT VOXEL-BASED BRAIN NETWORKS ANALYSIS

Yu Wang, Mo Xu, Ling Ren, Xiaorui Zhang, Di Wu, Huazhong Yang - *Tsinghua Univ.*
Yong He - *Beijing Normal Univ.*
Ningyi Xu - *Microsoft Research Asia*

SESSION

8B Room: Fir Ballroom 8:30 - 10:00am

Advances in Debugging and Simulation

MODERATOR(S):

Pankaj Chauhan - *Calypto Design Systems, Inc.*
Sanjit A. Seshia - *Univ. of California, Berkeley*

This session contains three papers addressing problems in debugging and simulation. The first paper proposes a new SAT-based approach to debugging RTL designs. The second paper describes a simulation-based approach for improving observability in post-silicon debug. The last paper presents a new approach for constrained random simulation.

8B.1 DEBUGGING WITH DOMINANCE: ON-THE-FLY RTL DEBUG SOLUTION IMPLICATIONS

Hratch Mangassarian, Andreas Veneris - *Univ. of Toronto*
Duncan Exon Smith, Sean Safarpour - *Vennsa Technologies, Inc.*

8B.2 SIMULATION-BASED SIGNAL SELECTION FOR STATE RESTORATION IN SILICON DEBUG

Debapriya Chatterjee, Calvin McCarter, Valeria Bertacco - *Univ. of Michigan*

8B.3 TOWARD AN EXTREMELY-HIGH-THROUGHPUT AND EVEN-DISTRIBUTION PATTERN GENERATOR FOR THE CONSTRAINED RANDOM SIMULATION TECHNIQUES

Bo-Han Wu, Chun-Ju Yang, Chia-Cheng Tso, Chung-Yang (Ric) Huang - *National Taiwan Univ.*

SESSION 8C

Room: Pine Ballroom **8:30 - 10:00am**

System-level Power Management

MODERATOR(S):

Sheldon Tan - *Univ. of California, Riverside*

This session presents papers that address power management and optimization in multi-core processors, multi-processor System-on-Chip (MPSoC) architectures, and hybrid storage systems. The first paper focuses on dynamically identifying the optimal threads and voltage/frequency settings for parallel workloads. The second paper discusses dynamic power management techniques for pipelined MPSoCs architectures aimed at multi-media applications such as H.264 code. The final paper in this session discusses techniques for dynamically reconfiguring electrical energy storage systems with an objective of maximizing the cycle efficiency and capacity utilization of a hybrid power supply system.

8C.1 IDENTIFYING THE OPTIMAL ENERGY-EFFICIENT OPERATING POINTS OF PARALLEL WORKLOADS

Can Hankendi, Ayse Coskun - *Boston Univ.*

Ryan Cochran, Sherief Reda - *Brown Univ.*

8C.2 SYSTEM-LEVEL APPLICATION-AWARE DYNAMIC POWER MANAGEMENT IN ADAPTIVE PIPELINED MPSOCS FOR MULTIMEDIA

Haris Javaid, Sri Parameswaran - *Univ. of New South Wales*

Muhammad Shafique, Jörg Henkel - *Karlsruher Institut für Technologie*

8C.3 BALANCED RECONFIGURATION OF STORAGE BANKS IN A HYBRID ELECTRICAL ENERGY STORAGE SYSTEM

Younghyun Kim, Sangyoung Park, Naehyuck Chang - *Seoul National Univ.*

Yanzhi Wang, Qing Xie, Massoud Pedram - *Univ. of Southern California*

Massimo Poncino - *Politecnico di Torino*

SPECIAL SESSION

6S

Room: Oak Ballroom **10:30am - 12:30pm**

2011 TAU Power Grid Simulation Contest

MODERATOR(S):

Sani Nassif - *IBM Corp.*

ORGANIZER(S):

Zhuo Li - *IBM Corp.*

The power grid is a critical component of today's digital VLSI designs. Verification of these large-scale on-chip power delivery networks is essential to ensuring the final design's correct functionality. To spur academic research in this vital verification step, the IBM Austin Research Lab, with support from the ACM TAU Workshop, has successfully organized the first annual TAU Power Grid Simulation Contest, with ten university teams across the world participated.

This special session starts with the overview of the contest and the release of new IBM benchmarks. The top three wining teams will then disclose the methods/techniques they applied to successfully tackle these large scale industrial power grid designs.

6S.1 2011 TAU POWER GRID SIMULATION CONTEST: BENCHMARK SUITE AND RESULTS
Zhuo Li, Frank Liu, Sani Nassif - *IBM Research - Austin*
Raju Balasubramanian - *IBM Systems and Technology Group,*

6S.2 POWERRUSH: A LINEAR SIMULATOR FOR POWER GRID
Jianlei Yang, Zuowei Li, Yici Cai, Qiang Zhou - *Tsinghua Univ.*

6S.3 FAST STATIC ANALYSIS OF POWER GRIDS: ALGORITHMS AND IMPLEMENTATIONS
Zhiyu Zeng, Tong Xu, Peng Li - *Texas A&M Univ.*
Zhuo Feng - *Michigan Technological Univ.*

6S.4 ON THE PRECONDITIONER OF CONJUGATE GRADIENT METHOD - A POWER GRID SIMULATION PERSPECTIVE
Chung-Han Chou, Nien-Yu Tsai, Hao Yu, Che-Rung Lee,
Shih-Chieh Chang - *National Tsing Hua Univ.*
Yiyu Shi - *Missouri Univ. of Science and Technology*

SESSION

9A

Room: Fir Ballroom **10:30am - 12:30pm**

Advances in Clocking and Routing for ASIC and On-Chip Communication

MODERATOR(S):

Shiyan Hu - *Michigan Technological Univ.*
Evangeline Young - *The Chinese Univ. of Hong Kong*

This session has four interesting papers on clocking and routing. The first paper develops a new non-tree topology that fuses clock trees to create large-scale redundancy in a clock network. The second paper proposes to reduce clocking power through using pulsed latches and pulsed registers. The third paper describes an innovative method to use adjustable delay buffers to construct a tunable clock tree for assigning useful skews under different power modes. The last paper in session presents a novel topology synthesis algorithm based on shortest path Steiner arborescence for on-chip interconnect networks.

9A.1 MULTILEVEL TREE FUSION FOR ROBUST CLOCK NETWORKS
Myung-Chul Kim, Dong-Jin Lee, Igor L. Markov - *Univ. of Michigan*

9A.2 IMPLEMENTATION OF PULSED-LATCH AND PULSED-REGISTER CIRCUITS TO MINIMIZE CLOCKING POWER
Seungwhun Paik, Youngsoo Shin - *KAIST*
Gi-Joon Nam - *IBM Research - Austin*

9A.3 USEFUL-SKEW CLOCK OPTIMIZATION FOR MULTI-POWER MODE DESIGNS
Hsuan-Ming Chou, Hao Yu, Shih-Chieh Chang - *National Tsing Hua Univ.*

9A.4 ATREE-BASED TOPOLOGY SYNTHESIS FOR ON-CHIP NETWORK
Bo Yuan, Jason Cong, Yuhui Huang - *Univ. of California, Los Angeles*

SESSION 9B

Room: Pine Ballroom — 10:30am - 12:30pm

Frontiers in Verification

MODERATOR(S):

Sanjit A. Seshia - *Univ. of California, Berkeley*
Pankaj Chauhan - *Calypto Design Systems, Inc.*

This session contains five papers spanning a range of topics in formal verification and simulation. The first paper addresses the important problem of verifying locking in phase-locked loops. The second paper considers the problem of verifying circuits that perform approximate computing. The third paper describes a new property-specific approach to SAT-based model checking. The fourth paper presents results on formal verification of multithreaded microprocessor designs, while the last paper proposes a way to speed up simulation using GPUs.

9B.1* FORMAL VERIFICATION OF PHASE-LOCKED LOOPS USING REACHABILITY ANALYSIS AND CONTINUIZATION
Matthias Althoff, Akshay Rajhans, Bruce H. Krogh, Soner Yaldiz, Xin Li, Larry Pileggi - *Carnegie Mellon Univ.*

9B.2 MACACO: MODELING AND ANALYSIS OF CIRCUITS FOR APPROXIMATE COMPUTING
Rangharajan Venkatesan, Amit Agarwal, Kaushik Roy, Anand Raghunathan - *Purdue Univ.*

9B.3 PROPERTY-SPECIFIC SEQUENTIAL INVARIANT EXTRACTION FOR SAT-BASED UNBOUNDED MODEL CHECKING
Hu-Hsi Yeh, Cheng-Yin Wu, Chung-Yang (Ric) Huang - *National Taiwan Univ.*

9B.4S AUTOMATIC FORMAL VERIFICATION OF MULTITHREADED PIPELINED MICROPROCESSORS
Miroslav Velev, Ping Gao - *Aries Design Automation, LLC*

9B.5S ACCELERATING RTL SIMULATION WITH GPUS
Hao Qian, Yangdong Deng - *Tsinghua Univ.*

SESSION 9C

Room: Cedar Ballroom — 10:30am - 12:30pm

System-level Power and Thermal Estimation

MODERATOR(S):

Jörg Henkel - *Karlsruher Institut für Technologie*
Sri Parameswaran - *Univ. of New South Wales*

The papers in this session address topics in system-level power and thermal estimation. The first paper extends the classical power, area, and timing modes in CACTI to include accurate leakage power estimation and to model leakage power reduction techniques. It also examines the impact of power gating on multi-level caches. The next paper presents an innovative approach for compressing RTL simulation traces that are widely utilized for power estimation. The third paper is somewhat of a counterpoint, presenting a theoretical framework for dynamic power estimation. The final paper in this session presents approaches for estimating and predicting die temperatures under power measurement inaccuracies and limited thermal sensors.

9C.1* CACTI-P: ARCHITECTURE-LEVEL MODELING FOR SRAM-BASED STRUCTURES WITH ADVANCED LEAKAGE REDUCTION TECHNIQUES
Sheng Li, Norman P. Jouppi - Hewlett-Packard Labs.
Ke Chen - Univ. of Notre Dame and Hewlett-Packard Labs.
Jung Ho Ahn - Seoul National Univ.
Jay B. Brockman - Univ. of Notre Dame

9C.2 A TRACE COMPRESSION ALGORITHM TARGETING POWER ESTIMATION OF LONG BENCHMARKS
Andrey Ayupov, Steven Burns - *Intel Corp.*

9C.3 A THEORETICAL PROBABILISTIC SIMULATION FRAMEWORK FOR DYNAMIC POWER ESTIMATION
Markus Olbrich, Lei Wang, Erich Barke - *Leibniz Univ. Hannover*
Thomas Büchner, Markus Bühler, Philipp Panitz - *IBM Corp.*

9C.4 FULL-CHIP RUNTIME ERROR-TOLERANT THERMAL ESTIMATION AND PREDICTION FOR PRACTICAL THERMAL MANAGEMENT
Hai Wang, Sheldon X.-D. Tan, Guangdeng Liao - *Univ. of California, Riverside*
Rafael Quintanilla, Ashish Gupta - *Intel Corp.*

All speakers are denoted in bold | S - denotes short paper | * - denotes best paper candidate

TUTORIAL

3T

Room: Oak Ballroom 2:00 - 4:00pm

Emerging Nonvolatile Memory and Memristors

MODERATOR(S):

Yiran Chen - *Univ. of Pittsburgh*

ORGANIZER(S):

Yiran Chen - *Univ. of Pittsburgh*

In this session, we invited four prestigious speakers from both industry and research institute to share their insights on emerging non-volatile memory technologies and their impacts on the electronic design and design automations. The first talk by Dr. Huai from Avalanche Technology will give an overview of STT-RAM technologies, including the current research status and future prospects. The second talk by Dr. Joshi from IBM T. J. Watson will present a case study on the statistical analysis of emerging memory designs. The third talk by Dr.Prenat from Spintec will deal with MRAM modeling and design tools, and their applications in developing non-volatile logic circuits. In the fourth talk, Dr. Ribeiro from HP Labs will share their latest development progress and understanding on memristor devices.

3T.1 PROGRESS AND OUTLOOK FOR STT-MRAM
Yiming Huai, Yuchen Zhou, Ioan Tudosa, Roger Malmahall, Rajiv Ranjan, Jing Zhang - *Avalanche Technology*

3T.2 UNIVERSAL STATISTICAL CURE FOR PREDICTING MEMORY LOSS
Rajiv Joshi - *IBM T.J. Watson Research Ctr.*
Rouwaida Kanj - *IBM Research - Austin*
Peiyuan Wang - *Univ. of Pittsburgh*
Hai (Helen) Li - *Polytechnic Institute of New York Univ.*

3T.3 HYBRID CMOS/MAGNETIC PROCESS DESIGN KIT AND APPLICATION TO THE DESIGN OF HIGH-PERFORMANCES NON-VOLITILE LOGIC CIRCUITS
Guillaume Prenat, Bernard Dieny, Jean-Pierre Nozierez - *Spintec*
Gregory DiPendina, Kholdoun Torki - *IMAG federation*

3T.4 PROGRESS IN CMOS-MEMRISTOR INTEGRATION
Gilberto Medeiros Ribeiro, Janice H. Nickel, J. Joshua Yang - *Hewlett-Packard Labs.*

SESSION

10A

Room: Fir Ballroom 2:00 - 4:00pm

Advanced Timing and Power Optimizations in Physical Design

MODERATOR(S):

Tsung-Yi Ho - *National Cheng Kung Univ.*
Masanori Hashimoto - *Osaka Univ.*

This session consists of four papers addressing advanced timing and power optimizations in physical design. The first paper in this session proposes a graph based timing model and a Lagrangian relaxation based formulation which can decouple timing analysis from optimization in gate sizing and device technology selection. The second paper describes a novel urgent path guided algorithm for gate sizing and mechanical stress optimization. The third paper proposes a polynomial time approximation scheme for the peak power driven voltage partitioning problem. The last paper presents an innovative timing ECO optimization technique considering the smoothness of timing critical paths.

10A.1* GATE SIZING AND DEVICE TECHNOLOGY SELECTION ALGORITHMS FOR HIGH-PERFORMANCE INDUSTRIAL DESIGNS
Muhammet Mustafa Ozdal, Steven Burns - *Intel Corp.*
Jiang Hu - *Texas A&M Univ.*

10A.2 IMPROVING DUAL V$_t$ TECHNOLOGY BY SIMULTANEOUS GATE SIZING AND MECHANICAL STRESS OPTIMIZATION
Lin Yuan - *Synopsys, Inc.*
Junjun Gu, Gang Qu - *Univ. of Maryland*
Cheng Zhuo - *Univ. of Michigan*

10A.3 THE APPROXIMATION SCHEME FOR PEAK POWER DRIVEN VOLTAGE PARTITIONING
Shiyan Hu, Jia Wang, Xiaodao Chen, Chen Liao - *Michigan Technological Univ.*

10A.4 TIMING ECO OPTIMIZATION VIA BÉZIER CURVE SMOOTHING AND FIXABILITY IDENTIFICATION
Hua-Yu Chang, Yao-Wen Chang - *National Taiwan Univ.*
Iris Hui-Ru Jiang - *National Chiao Tung Univ.*

SESSION 10B

Room: Pine Ballroom 2:00 - 4:00pm

Test Cost and Quality

MODERATOR(S):

Mango Chia-Tso Chao - *National Chiao Tung Univ.*

This session covers various topics in test cost and quality. The first paper proposes an unified test-data-compression approach with low-cost decompression architecture for low pin-count interface for multi-core SoCs. The second papers presents a methodology for enhancing post-silicon debugging, based on tracking the toggle count of top-level control signals. The third paper proposes a method for predicting the effectiveness of alternate RF tests by pass/fail metric estimation using non-parametric kernel density estimation for On-Chip RF Built-in Tests. The fourth paper proposes a new time-efficient framework for evaluating test quality (FETQ) that uses tester data from normal production. The last paper describes how a clock skew-tuning circuit can be made resilient to process variations using a hierarchical tuning algorithm.

10B.1 TEST-DATA VOLUME AND SCAN-POWER REDUCTION WITH LOW ATE INTERFACE FOR MULTI-CORE SOCS

Xrysovalantis Kavousianos, Vasileios Tenentes - *Univ. of Ioannina*

10B.2 POST-SILICON BUG DIAGNOSIS WITH INCONSISTENT EXECUTIONS

Andrew DeOrio, Daya Shanker Khudia, Valeria Bertacco - *Univ. of Michigan*

10B.3 ON PROVING THE EFFICIENCY OF ALTERNATIVE RF TESTS

Nathan Kupp - *Yale Univ.*

Haralampos Stratigopoulos - *TIMA Laboratory/CNRS*

Petros Drineas - *Rensselaer Polytechnic Institute*

Yiorgos Makris - *Univ. of Texas, Dallas*

10B.4S STATISTICAL DEFECT-DETECTION ANALYSIS OF TEST SETS USING READILY-AVAILABLE TESTER DATA

R. D. (Shawn) Blanton, Xiaochun Yu - *Carnegie Mellon Univ.*

10B.5S A ROBUST ARCHITECTURE FOR POST-SILICON SKEW TUNING

Mac Y.C. Kao, Kun-Ting Tsai, Shih-Chieh Chang - *National Tsing Hua Univ.*

SESSION 10C

Room: Cedar Ballroom 2:00 - 4:00pm

New Techniques for System-level Communication Synthesis and Hardware Metering

MODERATOR(S):

Prabhat Mishra - *Univ. of Florida*

The first two papers in this session address the issue of communication design for NoC architectures. The first paper presents an automated layout generation methodology and tools for low-swing crossbars for NOC based systems implementations. The second talk introduces an interesting approach to optimize the performance/power and cost trade-off in NoCs, by using a hybrid scheme in which two types of routers exist: buffered and non-buffered. The authors of the third paper try to optimize the synchronous elasticization concept of design. They do this by proposing a mechanism to identify and selectively replace area/power hungry eager forks (EForks) with simple USForks. The last paper presents an approach for uniquely identifying ICs by measuring the power consumption and threshold voltages for specific gates within the circuit. This passive metering approach is resilient to the effects of aging.

10C.1 A LOW-SWING CROSSBAR AND LINK GENERATOR FOR LOW-POWER NETWORKS-ON-CHIP

Chia-Hsin Owen Chen, Sunghyun Park, Tushar Krishna, Li-Shiuan Peh - *Massachusetts Institute of Technology*

10C.2 EXPLORING HETEROGENEOUS NOC DESIGN SPACE

Hui Zhao, Mahmut Kandemir, Wei Ding, Mary Jane Irwin - *Pennsylvania State Univ.*

10C.3 SYNCHRONOUS ELASTICIZATION AT A REDUCED COST: UTILIZING THE ULTRA SIMPLE FORK AND CONTROLLER MERGING

Eliyah Kilada, Kenneth S. Stevens - *Univ. of Utah*

10C.4 ROBUST PASSIVE HARDWARE METERING

Sheng Wei, Miodrag Potkonjak - *Univ. of California, Los Angeles*

Ani Nahapetian - *Univ. of California, Los Angeles and California State Univ., Northridge*

PANEL

2P Room: Oak/Fir Ballroom 4:30 - 5:30pm

Manycore, Heterogeneous, or Neither: Which One is the Way to Go for EDA?

ORGANIZER(S):

Rasit O. Topaloglu - *GLOBALFOUNDRIES*

PANELIST(S):

Bevan Baas - *Univ. of California, Davis*
Sunil P. Khatri - *Texas A&M Univ.*
Patrick H. Madden - *SUNY Binghamton*
Ramesh Narayanaswamy - *Synopsys, Inc.*
Duaine Pryor - *Mentor Graphics Corp.*
Gary Smith - *Gary Smith EDA*
Tom Syprou - *Advanced Micro Devices, Inc.*

Computing industry is transitioning into manycore and heterogeneous architectures. While EDA has been fast to adapt to multicores, transitioning to GPUs have not been fast-paced. This has been due to cost, programming, and performance considerations. As there are research examples of success for EDA algorithms in GPUs, it is an interesting question to answer whether EDA could also take advantage of upcoming manycore and heterogeneous architectures. This panel brings together experts from academia and industry to discuss feasibility of implementing EDA algorithms in such new architectures. Audience will have a chance to ask questions to the panelists.

WORKSHOP

1W Room: Oak Ballroom 9:00am - 5:00pm

IEEE/ACM Workshop on Variability Modeling and Characterization

ORGANIZER(S):

Hidetoshi Onodera - *Kyoto Univ.*
Frank Liu - *IBM Corp.*
Kevin Cao - *Arizona State Univ.*

SPEAKER(S):

Rob Aitken - *ARM, Inc.*
Luigi Capodeici - *GLOBALFOUNDRIES*
Vijay Reddy - *Texas Instruments, Inc.*
Takayasu Sakurai - *Univ. of Tokyo*
Kiyoshi Takeuchi - *Renesas Electronics Corp.*
Gilson Wirth - *Univ. Federal do Rio Grande do Sul*

It is widely recognized that variability is emerging as a fundamental challenge to IC design in scaled CMOS technology; and it will have profound impact on nearly all aspects of circuit performance. While some of the negative effects of variability can be handled with improvements in the manufacturing process, the industry is starting to accept the fact that some of the effects are better mitigated during the design process. Handling variability in the design process will require accurate and appropriate models of variability and its dependence on designable parameters (i.e. layout), and its spatial and temporal distributions. It also requires carefully designed test structures and proper statistical data analysis methods to extract meaningful models from large volumes of silicon measurements.

The resulting compact modeling of systematic, random, spatial, and temporal variations is essential to abstract the physical level variations into a format the designers (and more importantly, the tools they use) can utilize. This workshop provides a forum to discuss current practice as well as near future research needs in test structure design, variability characterization, compact variability modeling, and statistical simulation.

Key Topics

- Physics mechanisms and technology trends of device-level variations
- First-principles simulation methods for predicting variability
- Time-dependent variation and their interaction with other variation sources
- Compact modeling of variations in devices and interconnect
- Device and circuit level modeling techniques
- Test structure design for variability
- Variability characterization, bounding and extraction
- Statistical data analysis and model extraction methods
- Novel implementation and simulation techniques for dealing with variability

Please visit the workshop website http://nimo.asu.edu/vmc/ for more up-to-date information.

WORKSHOP

2W Room: Fir Ballroom 9:00am - 5:00pm

International Workshop on Adaptive Power Management with Machine Intelligence

ORGANIZER(S):
Massoud Pedram - *Univ. of Southern California*
Luca Benini - *Univ. di Bologna*
Ayse Coskun - *Boston Univ.*
Qinru Qiu - *Syracuse Univ.*

SPEAKER(S):
Mohamed M. Sabry - *Ecole Polytechnique Fédérale de Lausanne*
Jürgen Teich - *Univ. of Erlangen-Nuremberg*
Andrea Acquaviva - *Politecnico di Torino*
Naehyuck Chang - *Seoul National Univ.*
Karthik Kumar - *Intel Corp.*
Sehwan Kim - *Univ. of California, Irvine*
Lide Zhang - *Univ. of Michigan*
Zhikui Wang - *Hewlett-Packard Co.*
Pradip Bose - *IBM Corp.*
Paul Bogdan - *Carnegie Mellon Univ.*

It is reported by the U.S. Environmental Protection Agency that in order for the U.S. to keep a sustained growth, it is important to curb its energy use and carbon emission. Particular effort is needed to control the power and energy consumption of IT facilities, from computing clusters, data centers, desktop and laptop computers, to consumer electronics. Effective power management will help to relieve the power bottleneck of today's VLSI design and accelerate the growth of the information technology industries.

A robust power management system should be able to work on different types of hardware with variable workload. The ability to adapt to the environment is the key to maintain its efficiency. Artificial intelligence techniques such as machine learning, data classification and pattern recognition have recently been successfully applied in many applications from autonomous resource management to adaptive architecture reconfiguration. The integration of low power techniques with machine intelligence will lead to a new research direction that leads to autonomous power optimization with minimum user intervenes.

This workshop aims at providing a forum for academia researchers and industrial experts to discuss issues and exchange research advances on adaptive power optimization and resource management using machine intelligence approaches. It will also provide a communication channel between engineers in computer aided design and experts in artificial intelligence to facilitate cross-domain collaboration.

More detailed information of the workshop can be found at:
http://www.bu.edu/peaclab/apmmi11/

WORKSHOP

3W Room: Pine Ballroom 9:00am - 5:00pm

Seventh International Workshop on Constraints in Formal Verification (CFV'11)

ORGANIZER(S):

Miroslav N. Velev (Chair) - *Aries Design Automation, LLC*
Maciej Ciesielski - *Univ. of Massachusetts*
Masahiro Fujita - *Univ. of Tokyo*
Alex Groce - *Oregon State Univ.*
Daniel Grosse - *Univ. of Bremen*
Michael Hsiao - *Virginia Polytechnic Institute and State Univ.*
Sumit Jha - *Univ. of Central Florida*
Robert Jones - *Intel Corp.*
Peter-Michael Seidel - *Advanced Micro Devices, Inc.*
Andreas Veneris - *Univ. of Toronto*
Markus Wedler - *Univ. of Kaiserslautern*

SPEAKER(S):

Carl Seger - *Intel Corp.*
Natarajan Shankar - *SRI*

Formal verification is of crucial significance in the development of hardware and software systems. In the last few years, tremendous progress was made in both the speed and capacity of constraint technology. Most notably, SAT solvers have become orders of magnitude faster and capable of handling problems that are orders of magnitude bigger, thus enabling the formal verification of more complex computer systems.

As a result, the formal verification of hardware and software has become a promising area for research and industrial applications. The main goals of the Constraints in Formal Verification workshop are to bring together researchers from the CSP/SAT and the formal verification communities, to describe new applications of constraint technology to formal verification, to disseminate new challenging problem instances, and to propose new dedicated algorithms for hard formal verification problems. This workshop will be of interest to researchers from both academia and industry, working on constraints or on formal verification, and interested in the application of constraints to formal verification.

The scope of the workshop includes topics related to the application of constraint technology to formal verification, namely:
1) application of constraint solvers to hardware verification
2) application of constraint solvers to software verification
3) dedicated solvers for formal verification problems
4) challenging formal verification problems

WORKSHOP

4W Room: Cedar Ballroom 9:00am - 5:00pm

Nanolithography & IC Design/CAD in Extreme Scaling: What, Why, and How?

ORGANIZER(S):
David Z. Pan - *Univ. of Texas, Austin*
Kevin Lucas - *Synopsys, Inc.*
Vivek Singh - *Intel Corp.*

SPEAKER(S):
Bill Arnold - *ASML*
Lars Bomholt - *Synopsys Switzerland LLC*
Martin Burkhardt - *IBM Corp.*
Jack Chen - *Taiwan Semiconductor Manufacturing Co., Ltd.*
Andrew B. Kahng - *Univ. of California at San Diego*
Harry Levinson - *GLOBALFOUNDRIES*
Soichi Owa - *Nikon Corp.*
Moshe Preil - *GLOBALFOUNDRIES*
Sam Sivakumar - *Intel Corp.*
Andres J. Torres - *Mentor Graphics Corp.*

Continuing the CMOS scaling in deep submicron always seems "mission impossible." However, the semiconductor industry in the last 45 years has shown the world "yes, we can." It is amazing to see that the 193nm lithography has been pushed all the way to 22nm, and it is likely to be further extended to 14nm node using double/triple patterning technologies. Beyond 14nm, the leading candidates include multiple (e.g., triple/quadruple) patterning lithography, EUV lithography, E-beam direct-write, and other maskless lithography.

So, how many more tricks are left in lithographer's bag? At what cost? Is it still worthwhile to scale and why (not)? What are the new design requirements, and how EDA industry shall respond?

In this one-day workshop, leading experts are invited to shed light on "what, why and how" of various enabling nanolithography technologies and their implications on IC design and EDA tools/methodologies.

The invited talks will be organized around three sessions:
(1) double/multiple patterning lithography
(2) EUVL
(3) E-beam and maskless lithography.

There will be a poster session for open discussions and showcase of recent/early results.

CANDE WORKSHOP

Room: Siskiyou Ballroom **8:00am - 6:00pm**

The CANDE (Computer-Aided Network Design) Committee is a technical activity of the IEEE Circuits and Systems Society and IEEE Council on Electronic Design Automation which acts as a working group for electronic computer-aided design. The CANDE Committee holds a yearly workshop to discuss advanced issues relevant to the CAD community, bringing together practitioners, researchers, and managers from industry and academia.

Workshop Schedule

8:00-8:25 Breakfast

8:25-8:30 Opening Remarks

8:30-9:30 Session I: Sense and Sensibility
Title: Using Infrared Imaging to Improve IC Design
Sherief Reda, Brown University

Title: Synthesizing Logical Computation on Stochastic Bit Streams for Sensing Applications
Marc Riedel, University of Minnesota, Twin Cities

9:30-10:00 Special Session: Student Research Highlights

10:00-10:30 Coffee Break + Poster Session

10:30-12:00 Session II: GPU for EDA Computing
Title: EDA Computing with OpenCL for GPU Architectures and Beyond
Rasit Onur Topaloglu, GLOBALFOUNDRIES, Inc.

Title: Leveraging GPU Computing for VLSI CAD and Beyond
Peng Li, Texas A & M University

Title: GPU Evolution - Simplifying the Step to Heterogeneous Computing
Stephen Jones, NVIDIA, Inc.

12:00-1:15 Lunch and Lunch Keynote

1:15-3:00 Session III: Panel Discussion -- EDA Roadmap: Why and How?
Moderator: Farinaz Koushanfar, Rice University

Panelists:
Juan-Antonio Carballo, NetLogic Microsystems
Andrew B. Kahng, University of California at San Diego
Dave Noice, Cadence
Leon Stok, IBM

3:00-3:15 Coffee Break

3:15-4:15 Keynote Session
Title: Many-core GPU Computing - Current Victories and Coming Battles
Wen-Mei Hwu, University of Illinois, Urbana-Champaign

4:15-4:30 Coffee Break

4:30-5:30 Session IV: New FPGA Advances
Title: System-level Trends in FPGA Devices
Mike Hutton, Altera, Inc.

Title: Recent Advances in Xilinx FPGAs
Tim Tuan, Xilinx, Inc.

5:30-6:00 Evening Reception (sponsored by IEEE CEDA)

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Cadence Research Labs
2150 Shattuck Ave., 10th Fl.
Berkeley, CA 94704
510-647-2804
jrp@cadence.com

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Technische Univ. München
Institute for Electronic Design Automation, Arcisstr. 21
Munich, 80333 Germany
+49-89-289-23679
graeb@tum.de

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Shinji Kimura
Waseda University
2-7 Hibikino, Wakamatsu,
Kitakyushu, 808-0135 Japan
+81-93-692-5374
shinji_kimura@waseda.jp

CONFERENCE MANAGER
Kathy Embler
MP Associates, Inc.
1721 Boxelder St., Ste. 107
Louisville, CO 80027
303-530-4562
kathy@mpassociates.com

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Janelia Farms Research Campus
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571-209-4151
schefferl@janelia.hhmi.org

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Karlsruhe Institute of Technology (KIT)
Kaiserstr. 12, Bldg. 20.20
Karlsruhe, 76131 Germany
+49-608-721-6050
henkel@kit.edu

ACM/SIGDA REPRESENTATIVE
Massoud Pedram
Univ. of Southern California
EE Building, Rm. 344
3740 McClintock Ave.
Los Angeles, CA 90089
213-740-4458
pedram@usc.edu

PROGRAM CHAIR
Alan J. Hu
Dept. of Computer Science
Univ. of British Columbia
2366 Main Mall,
Vancouver, BC V6T 1Z4, Canada
604-822-6667
ajh@cs.ubc.ca

EUROPEAN REPRESENTATIVE
Andreas Herkersdorf
Technische Universitaet Muenchen
Institute for Integrated Systems
Arcisstr. 21
Munich, 80333 Germany
+49-89-289-22515
herkersdorf@tum.de

CEDA REPRESENTATIVE
Andreas Kuehlmann
Coverity, Inc.
185 Berry St., Ste. 1600
San Francisco, CA 94107
415-321-5233
akuehlmann@coverity.com

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Monday, November 7	7:30am - 8:30am
Tuesday, November 8	7:30am - 8:30am
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